SIMULATION OF A NONLINEAR GAAS MESFET MODEL FOR USE IN THE DESIGN OF NONLINEAR MICROWAVE CIRCUITS

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ABSTRACT

A computer program has been developed that performs a large-signal simulation of a GaAs Metal-Semiconductor-Field-Effect-Transistor (MESFET) using the Curtice-Ettenberg model [1]. The model is then used to design non-linear microwave circuits such as frequency multipliers and power amplifiers. The simulation employs a two-stage numerical approximation. The so called "multiple reflection" method, which is a special kind of "harmonic balance" technique, is used between the FET and the linear embedding network. The intrinsic FET with its nonlinearities is analyzed with Newton's method in the time domain. Comparison of simulation and experimental results of the designed circuit show good agreement.

INTRODUCTION

In the past decades the accurate modeling of microwave field effect transistors (FETs) has preoccupied the attention of many circuit designers. The modelling of the linear behavior of the FET is now a resolved problem. What still challenges the microwave circuit designer is the accurate modelling of the nonlinear behavior of the FET. Many researchers came up with different models; the Curtice-Ettenberg model [1], the Materka-Kacprzak mode [2], and the Raytheon model [3] are among the few. The purpose of this paper is to optimize one of these models to make them applicable in the design of optimum nonlinear microwave circuits such as frequency multipliers, mixers, and power amplifiers. The Curtice-Ettenberg model is used for the purpose because it is less complicated and requires less computation time. The simulation is done by separating the whole circuit into nonlinear and linear subcircuits and then analyzing it by the method of 'harmonic balance'. The idea of harmonic balance is to find a set of port voltage waveforms or harmonic voltage components that give the same currents in both the linear network equations and the nonlinear network equations; when that set is found, it must be the solution.

THE ANALYSIS METHOD

The harmonic balance approach is most useful for strongly or weakly nonlinear circuits that have single-tone excitation. It is widely applied to analyze microwave circuits such as frequency multipliers, power amplifiers and mixers subjected to local oscillator drive. In these circuits the harmonic balance technique usually consists of a time domain model of the GaAs FET coupled with the frequency domain models of the input and output matching networks. In other words, the harmonic balance method allows the use of multiport circuit theory [4] which can be used to simplify part of the circuit by lumping all the linear reactances, impedances, transmission lines, and other linear elements into a single matrix of limited size. By describing the linear part of the circuit as one multiport, it need be evaluated only once at each harmonic, with the results stored in matrices and no further evaluation is necessary. The model is illustrated in Fig. 1.

In reference to Fig. 1, since the currents in the linear and nonlinear sub-circuits must be equal the matrix Eq.(1) must be satisfied.

In Eq.(1) $I_{n,k}$ is a phasor quantity, the k^{th} harmonic component of the port n, calculated via the port voltages and the Y-matrix of the linear subcircuit; $\hat{I}_{n,k}$ is the current component calculated via the same port voltages and the nonlinear elements.

The circuit in Fig. 1 is successfully analyzed when either the steady-state voltage or current waveforms at each port are known. Alternatively, knowledge of the frequency components at all ports constitutes a solution because the frequency components and time waveforms are related by the Fourier series. If, for example, the frequency-domain port voltages

$$\begin{bmatrix} I_{1,0} \\ I_{1,1} \\ \cdot \\ \cdot \\ I_{1,K} \\ I_{2,0} \\ I_{2,1} \\ \cdot \\ \cdot \\ I_{2,K} \\ \cdot \\ \cdot \\ I_{N,K} \end{bmatrix} + \begin{bmatrix} \hat{I}_{1,0} \\ \hat{I}_{1,1} \\ \cdot \\ \cdot \\ \hat{I}_{1,K} \\ \hat{I}_{2,0} \\ \hat{I}_{2,1} \\ \cdot \\ \cdot \\ \hat{I}_{2,K} \\ \cdot \\ \cdot \\ \hat{I}_{N,K} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \cdot \\ \cdot \\ 0 \\ 0 \\ 0 \\ \cdot \\ \cdot \\ 0 \\ \cdot \\ \cdot \\ 0 \end{bmatrix} \quad (1)$$

are known, one can use the *Y*-parameter matrix for the linear subcircuit to find the port currents. The port currents can also be found by inverse Fourier transforming the voltages, to obtain their time-domain waveforms, and determining the current waveforms from the nonlinear elements.

The linear subcircuit can be treated as a multiport and described by its *Y*- or *S*- parameters. The nonlinear elements are modelled by their global *I/V* or *Q/V* characteristics and analyzed in the time domain [4]. In our case the FET constitutes the nonlinear subcircuitry and hence is analyzed in the time domain in order to simulate it accurately. On the other hand, the linear circuit response of the FET can be analyzed in the frequency domain. Transformation between the time and frequency domains is accomplished using a discrete Fourier Transform (DFT).

It must be noted that the equations for the nonlinear subcircuit are known only in the time domain and cannot be transformed to the frequency domain.

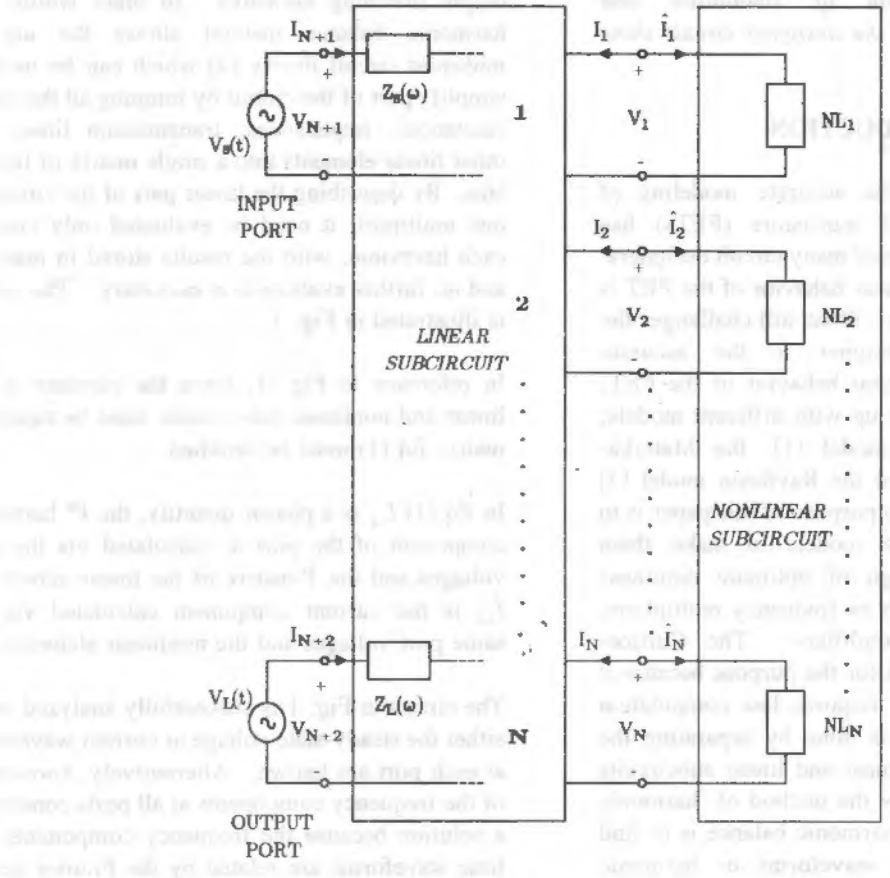

Figure 1 A Nonlinear Microwave Circuit, Divided into Linear and Nonlinear Subcircuits, with the Source and Load Impedances Absorbed into the Linear Subcircuit.

Thus, every voltage wave arriving at a port of the nonlinear subcircuit is transformed to the time domain using the Inverse Fast Fourier Transform (IFFT). After the time domain analysis of the nonlinear circuit voltages and currents, the results are transformed back to the frequency domain. It is to be noted that it is the intrinsic FET that makes up the nonlinear subcircuit. In reference to Figs. 2 and 3 (with $Z_1 = Z_2 = Z_L$, the intrinsic FET can be analyzed using the following network equations.

$$\frac{2v_1^i - v_{gs}}{Z_L} - i_{gs} - i_{gd} - \frac{dQ_{gs}}{dt} - \frac{dQ_{gd}}{dt} = 0 \tag{2}$$

$$\frac{2v_2^i - v_{ds}}{Z_L} - i_{ds} + i_{dg} + \frac{dQ_{gd}}{dt} = 0 \tag{3}$$

$$\frac{V_j - v_{gs}}{R_i} + \frac{dQ_{gs}}{dt} = 0 \tag{4}$$

where v_1^i and v_2^i are the incident voltages at ports 1 and 2, respectively. Q_{gs} and Q_{gd} are the charges stored in the gate-source and gate-drain junctions, respectively. For the actual computation, Eqs. (3) and (4) are rearranged and combined with Eq. (2) resulting in the following equations:

$$\frac{2v_1^i + 2v_2^i - 2v_{ds} - v_{dg}}{Z_l} + \frac{v_j - v_{ds} - v_{gd}}{R_i} = 0 \tag{5}$$

The voltages v_j, v_{ds}, and v_{gd} are taken as independent variables, while v_1^i and v_2^i are obtained from the reflection algorithm and they change at every iteration. The resulting system of $3n$ differential equations is discretized by approximating the time derivatives with secants through neighbouring samples as:

$$\frac{\partial v}{\partial t} \approx \frac{v(t + \Delta t) - v(t - \Delta t)}{2.\Delta t} \tag{6}$$

This leads to a system of nonlinear equations with $3n$ independent variables where n indicates the number of time domain samples. This system is solved by means of Newton's method as described below. All derivatives can be explicitly calculated and therefore by easily evaluated. Because the multiple reflection algorithm requires the equations to be solved many times with similar values, every iteration uses the previous solution as an initial guess. Only the very first iteration is supplied with a guess based on the DC components.

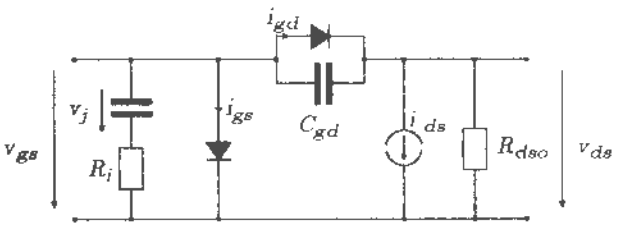

Figure 2 The Nonlinear Transistor Model

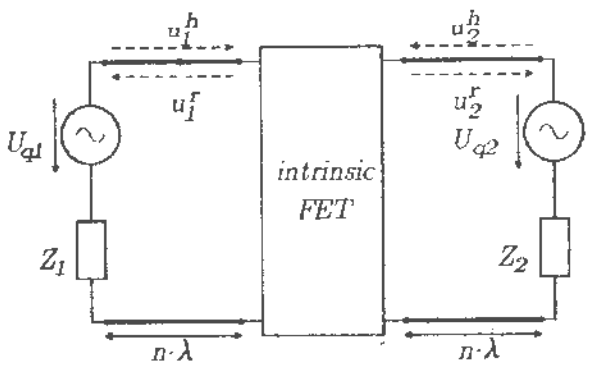

Figure 3 The Reflection Principle

NEWTON'S METHOD

The differential equations are discretized for all n samples forming the vector of independent variables as given in Eq. (7). On the other hand, the left sides of Eqs. (3), (4), and (5) are taken as components of a $3n$-dimensional vector error function F whose zero is found iteratively by the Newton's method. That is to say F can be expressed as shown in Eq. (8).

$$\vec{v} = \begin{bmatrix} v_j(t_1) \\ \cdot \\ \cdot \\ \cdot \\ v_j(t_n) \\ v_{gd}(t_1) \\ \cdot \\ \cdot \\ \cdot \\ v_{gd}(t_n) \\ v_2(t_1) \\ \cdot \\ \cdot \\ \cdot \\ v_2(t_n) \end{bmatrix} = \begin{bmatrix} v_1 \\ \cdot \\ \cdot \\ \cdot \\ v_n \\ v_n + 1 \\ \cdot \\ \cdot \\ \cdot \\ v_{2n} \\ v_{2n} + 1 \\ \cdot \\ \cdot \\ \cdot \\ v_{3n} \end{bmatrix} \tag{7}$$

$$F = \begin{bmatrix} \dfrac{2v_2^i - v_{ds}}{Z_L} - i_{ds} + i_{gd} + \dfrac{dQ_{gd}}{dt} \\ \dfrac{v_j - v_{gs}}{R_i} + \dfrac{dQ_{gd}}{dt} \\ \dfrac{2v_1^i + 2v_2^i - 2v_{ds} - v_{dg}}{Z_L} + \dfrac{v_j - v_{ds} - v_{gd}}{R_i} \\ - i_{ds} - i_{gs} \end{bmatrix} \tag{8}$$

Moreover, the updated voltage vector $\vec{v}+1$, is expressed as:

$$\vec{v}_{p+1} = \vec{v}_p - \left[\frac{\partial F}{\partial \vec{v}}\right]_p^{-1} F(\vec{v}_p) \tag{9}$$

where p indicates the iteration number.

Equation (6), which is used for discretization purpose, produces a Jacobian containing many zero elements as shown in Eq. (10) below.

$$\frac{\partial F}{\partial \vec{v}} = \begin{bmatrix} \dfrac{\partial F_1}{\partial v_1} & \dfrac{\partial F_1}{\partial v_2} & 0 & 0 & \dots & 0 & \dfrac{\partial F_1}{\partial v_n} & 0 & \dots \\ \dfrac{\partial F_2}{\partial v_1} & \dfrac{\partial F_2}{\partial v_2} & \dfrac{\partial F_2}{\partial v_3} & 0 & 0 & \dots & 0 & 0 & \dots \\ 0 & \dfrac{\partial F_3}{\partial v_2} & \dfrac{\partial F_3}{\partial v_3} & \dfrac{\partial F_3}{\partial v_4} & 0 & \dots & 0 & 0 & \dots \\ \vdots & \ddots & \ddots & \ddots & \ddots & \ddots & \ddots & \vdots & \dots \end{bmatrix} \tag{10}$$

The Jacobian is then inverted using the Gaussian elimination algorithm [5].

THE MULTIPLE REFLECTION ALGORITHM

As described earlier the harmonic balance method divides the network to be analyzed into linear and nonlinear subnetworks, which are connected at a number of ports. A solution is obtained when a set of port voltages causes a set of identical port currents into both the linear and the nonlinear subnetwork. In the particular case of a frequency doubler network, which is considered in this paper, one is only interested in a steady-state solution which can be obtained much faster by this method rather than by the time domain integration.

In the simulation the harmonic balance method is realized using the multiple reflection algorithm that requires no evaluation of derivatives and no initial guess. The method imitates the natural turn-on process of a circuit. Ideal transmission lines, which are a large integer multiple of the fundamental wave-length long, are assumed to exist between the two subnetworks (Fig. 3). On these lines the incident and reflected waves of the turn-on process are calculated. The reflected wave, $v_p^r(\omega)$, travelling back from the nonlinear subcircuit is multiplied by the frequency dependent reflection factor, $\Gamma(\omega)$, of the linear subnetwork and is added to the initial incident wave, $v_o^i(\omega)$, to give [4]:

$$v_p^i + 1(\omega) = v_o^i(\omega) + \Gamma(\omega) \cdot v_p^r(\omega) \tag{11}$$

where p indicates the iteration number.

The reflection factors of the linear subcircuit are given by:

$$\Gamma(\omega) = \frac{Z(\omega) - Z_L}{Z(\omega) + Z_L} \qquad (12)$$

Z_L is the characteristic impedance of the imaginary transmission lines between the subcircuits. Its choice is not so important, but fast convergence can be achieved if Z_L is approximately taken to be equal to $Z(\omega_0)$, i.e the port impedance of the circuit at the fundamental frequency.

For a rapid convergence of the algorithm the reflection factors at both ends of the transmission lines must be kept small. The DC bias sources, however, have an internal impedance of nearly zero. In this case a larger value of Z_s (source impedance) is assumed and the bias voltage V_{gs} is offset to compensate for this artificial increase in the DC source impedance. The flow diagram of the overall simulation is given in Fig. 4.

To determine the parameters of the Curtice-Ettenberg model one needs the DC as well as the S-parameter measurement results that describe the transistor. Neither of the two measurement results is sufficient alone to determine all the equivalent

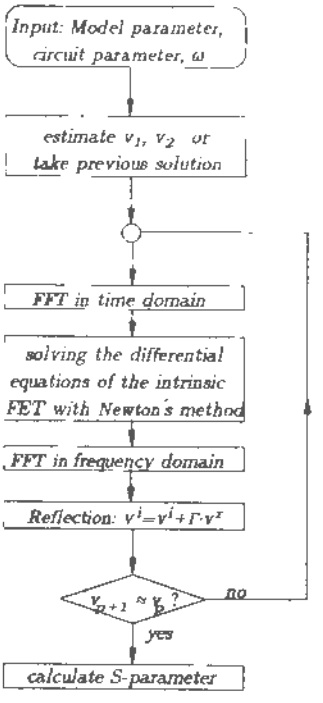

Figure 4 Flow Diagram of the Simulation

circuit elements shown in Fig. 2. This means both measurement results must be used and compared with the voltages and currents that are obtained during the simulation. Then, the model parameters are varied and with the help of an appropriate algorithm, the model is further optimized till a good agreement between simulation and measurement results is obtained. The algorithm used to optimize the model parameters of the FET is the so called 'evolution principle' and is well described in [6].

RESULTS

The model parameter extraction method described earlier has been applied to a GaAs MESFET type HLT dull-2. From the measured DC and *S*-parameters at 15 different operating points consisting of the combination: V_g {-15V, -0.5V,0.5V} and V_{ds} {0.5V, 1.0V, 1.5V, 3V, 5V}, and measured over the frequency range up to 40 GHz, the parameters of the Curtice-Ettenberg model have been extracted and given in Table 1. The relevant equations are as given in the Appendix section. Note that at first the parameters a_0, a_1, a_2, a_3, β and γ are determined from the DC measurements. By using these values and by varying τ,R_i, C_{gs0}, C_{gd0} and g_{min}, the curve-fitting between the measured and simulated *S*-parameters is performed.

Since the influence of the individual model parameters in some cases is interdependent with one another, it may be necessary to do several switching between the DC and *S*-parameter optimization cycles and search for optimum values and use different optimization variables at each stage. In other words, it is important to note that a_1, as an example, influences both the DC characteristics as well the small-signal transconductance gain and the paradox here is that the two optimization procedures do not always lead to the same value. For this reason both procedures must be interchangeably used to evaluate a_1 until a compromise value is found.

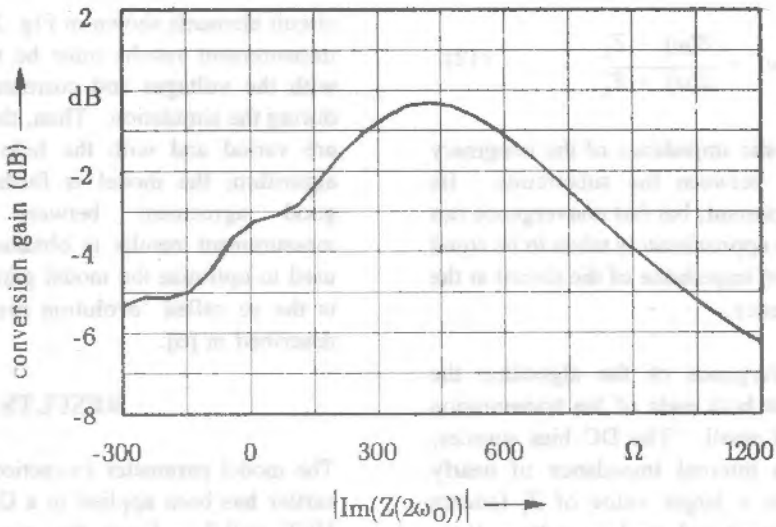

Figure 5 Calculated Maximum Achievable Conversion Gain of a 16 to 32 GHz Frequency Doubler Circuit as a Function of Second Harmonic Load Reactance.

Table 1: The extracted nonlinear model parameters of the HLT dull-2 GaAs FET.

a_o = 0.031520 A	a_1 = 0.060463 A/V	a_2 = 0.028680 A/V^2
a_3 = 0.00549 A/V^3	C_{gso} = 4.2072.10^{-13}F	C_{gdo} = 5.8223.10^{-14}F
R_i = 0.02742 Ω	V_{dso} = 2.5 V	V_T = 0.026 V
V_{bi} = 0.8 V	τ = 4.8867.10^{-12} s	g_{min} = 1.5.10^{-12} S
N = 1.5	I_s = 1.10^{-9} A	β = 0.04 1/V
F_C = 0.5	γ = 1.0675 1/V	

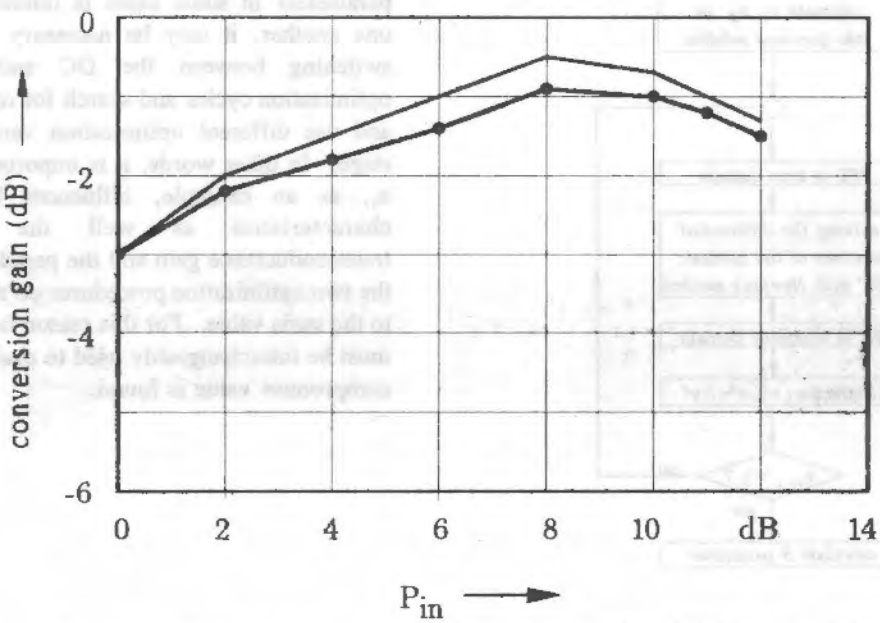

Figure 6 Measured and Simulated Conversion Gain of a 16 to 32 GHz Frequency Doubler Circuit as a Function of the Input Fundamental Power

The transistor model whose parameter extraction is shown above was used to design a 16 to 32 GHz frequency doubler. Figure 5 shows the predicted maximum achievable conversion gain of the doubler as a function of the second harmonic load reactance. The optimum load was found to be 120+j410 Ω. The measured and calculated conversion gain of the doubler as a function of the input power is given in Fig. 6. As can be seen from the figure there is good agreement between measurement and simulation results.

CONCLUSIONS

A simplified nonlinear GaAs MESFET model has been simulated and implemented for the design of nonlinear microwave circuits such as a frequency doubler. The harmonic balance technique has been used for the simulation. The designed circuit has been tested experimentally and proved to be in good agreement with the simulation results, thus verifying the validity of the approach used. The 16 to 32 GHz frequency doubler realized here has a maximum coverison gain of -0.5 dB which is quite a good result for such a high frequency of operation.

APPENDIX

The following equations for the nonlinear elements of the Cortice-Ettenberg mode [7] are implemented in the program:

a) Conduction current:

$$i_{ds} = \begin{cases} (a_0 + a_1 v_1 + a_2 v_1^2 + a_3 v_1^3)\tanh(\gamma v_{ds}) , & \text{for } v_{ds} \geq 0 \\ 0 , & \text{for } v_{ds} \leq 0 \end{cases} \qquad (A.1)$$

where:

$$v_1 = v_j(t-\tau)\ (1+\beta(V_{dso} - v_{ds})) \qquad (A.2)$$

In the simulation, τ is assumed to be zero.

b) Diode Currents:

$$i_{gs} = \begin{cases} I_s(\exp\left\{\frac{v_j}{NV_T}\right\} - 1)\ g_{\min} v_j , & \text{for } v_j \geq -5NV_T, \\ -I_s + g_{\min} v_j , & \text{for } -V_{br} + 50V_T \leq v_j < -5NV_T, \\ -I_s\left\{1 + \exp(-\frac{v_j + V_{br}}{V_T})\right\} + g_{\min} v_j , & \text{for } v_j \leq V_{br} + 50V_T, \end{cases} \qquad (A.3)$$

where,

$$V_T = \frac{kT}{q} \tag{A.4}$$

and

$$i_{ds} = \begin{cases} I_s\left(\exp\left[\dfrac{v_{gd}}{NV_T}\right] - 1\right) + g_{\min}v_{gd}\,, & \text{for } v_{gd} \geq -5NV_T, \\ -I_s + g_{\min}v_{gd}\,, & \text{for } -V_{br} + 50V_T < v_{gd} < -5NV_T, \\ -I_s\left[1 + \exp\left(-\dfrac{V_{gd} + V_{br}}{V_t}\right)\right] + g_{\min}v_{gd}\,, & \text{for } v_{gd} \leq -V_{br} + 50V_T, \end{cases} \tag{A.5}$$

where,

$$v_{gd} = v_{gs} - v_{ds} \tag{A.6}$$

Finally, the Schottky-contact capacitances are given by:

$$C_{gs} = \begin{cases} \dfrac{C_{gso}}{\sqrt{1 - \dfrac{v_j}{V_{bi}}}}\,, & \text{for } v_j < F_C V_{bi}, \\ \dfrac{C_{gso}}{\sqrt{1 - F_C}}\left[1 + \dfrac{v_j - F_C V_{bi}}{2V_{bi}(1 - F_C)}\right], & \text{for } v_j \geq F_C V_{bi}, \end{cases} \tag{A.7}$$

and

$$C_{gd} = \begin{cases} \dfrac{C_{gdo}}{\sqrt{1 - \dfrac{v_{gd}}{V_{bi}}}}\,, & \text{for } v_{gd} < F_C V_{bi}, \\ \dfrac{C_{gdo}}{\sqrt{1 - F_C}}\left[1 + \dfrac{v_{gd} - F_C V_{bi}}{2v_{bi}(1 - F_C)}\right], & \text{for } v_{gd} \geq F_C V_{bi} \end{cases} \tag{A.8}$$

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