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OPTIMISATION OF A MICROELECTRONIC ASSEMBLY PACKAGE USING RESPONSE SURFACE METHODOLOGY

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ABSTRACT
This article addressed heat conduction in microelectronics applications. ANSYS finite element design software was used to design the model, while Design Expert software was used for the response surface methodology (RSM) analysis. The components analysed were heat-sink base (HSB) thickness, thermal interface material (TIM) thickness, and chip thickness. A design of experiment comprising of 15 central composite design (CCD) for the coded levels (low (-) and high (+)) of the factors were generated. Heat flow was applied to the chip while a convective coefficient was applied to the heat-sink. The temperature solution was used to calculate the thermal resistance response for the 15 CCD experimental runs. The results from the RSM study proposed an optimal (minimization analysis) combination of 3.5 mm, 0.04 mm, and 0.75 mm, for HSB thickness, TIM thickness, and chip thickness respectively. While the optimal mean thermal resistance of 0.31052 K/W was achieved from the proposed optimal parameters.

Keywords: *RSM; CCD; thermal resistance; temperature; microelectronics*

1. INTRODUCTION

Heat management in microelectronics devices remain a challenge despite increased attention given to it. Most research works on managing heat in microelectronic devices centred their research on heat sink [1-4]. However, understanding how heat is conducted and managed in electronic packages are vital in the development of the components used in the assembly process. One of the ways to effectively dissipate heat from an electronic device is to ensure that the components used in the assembly process are of the right specification and quality. This could be achieved by making sure that the components used are optimised based on engineering specifications. There are different ways of optimising design specifications, but a lot of researchers [5 – 8] have used response surface methodology (RSM) and other optimisation methods to optimise components of different applications.

Oghenejoboh [9] used response surface methodology approach to analyse the Biosorption of nickel (II) ion from synthetic wastewater on watermelon rind activated carbon. The research established that response surface methodology is a vital tool for saving cost in the optimisation of adsorption process parameters. In another study by Leong *et al* [10], response surface methodology was used in the optimisation of flexible printed circuit board of electronics in the flow environment. The authors developed an empirical model using response surface methodology. The empirical model was used to optimise the process parameters which resulted in a maximum deflection and maximum stress of 0.402 mm and 0.582 MPa respectively.

Wang *et al* [11], did a study on a novel response surface method for design optimization of electronic packages. The research was based upon the fact that if too few sampling points or too many sampling points are used in RSM, it may lead to inaccurate results or expensive process respectively. The authors stated that RSM could be improved by their proposed sequential response surface refinement scheme couple Quasi-Monte Carlo sampling method. Gaston and Walton [12] researched on integrating simulation with response surface methodology in the optimisation of integrated circuit (IC) processes. The

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authors inferred that the combination of RSM and simulation is an extremely powerful concept in optimisation analysis and that it could be readily implemented by using available design of experiment (DOE) software.

In this study, response surface methodology (RSM) is employed for the optimisation of the required response [13, 14]. The second-order approximation function is used to describe the formulation of a response surface, and is represented mathematically as:

$$F(x) = a_o + \sum_{i=1}^{n_{dv}} b_i x_i + \sum_{i=1}^{n_{dv}} c_{ii} x_i^2 + \sum_{ij(i<j)}^{n_{dv}} c_{ij} x_i x_j \quad (1)$$

Where *F(x)* is the function or response approximated, $x_1 (i = 1, n_{dv})$ are the n_{dv} design variables, and (a_o, b_i, c_{ii}, c_{ij}) are the least-square fit coefficients [13].

Also, other researchers have conducted investigations on optimization of different parameters that could enhance thermal management in different applications [14, 15]. This investigation is aimed at proposing an optimal thermal resistance based on heat sink base (HSB) thickness, TIM thickness, and chip thickness.

2. MATERIALS AND METHOD

2.1 Experimental Design and Model Description

The components considered in this work are heat sink, thermal interface material (TIM), and flip chip. The three components are vital in heat generation and dissipation. In terms of assembling the components, the chip is mounted on the circuit board, while TIM is applied before mounting the heat sink. The chip is the heat generating device while the generated heat is dissipated through the TIM and heat sink to the environment. To effectively manage the thermal processes in the electronic package, it is necessary to have the right size of the components. To achieve the right size of components, it is advisable to employ optimisation.

This research work employs ANSYS for the development of the microelectronic assembly package (MAP). The initial dimensions of the developed model are given as: 10 mm x 10 mm x 0.5 mm for the chip, 10 mm x 10 mm x 0.035 mm for the TIM, and 30 mm x 30 mm x 2 mm for the heat sink base (HSB). In addition, there were ten (10) rectangular fins, each measuring 10 mm height, 30 mm length, and 1.5 mm width respectively. Figure 1 presents a schematic of the designed microelectronic assembly package.

In order to develop the design of experiment for the simulation runs, the Design Expert software was utilised. Montgomery [16] explained in detail the concept of design of experiment. In the present study, three factors were considered HSB thickness, TIM thickness, and flip chip thickness. The Design Expert coded levels of low (-) and high (+) were employed in the determination of the factors levels used in this investigation. Table 1 presents the MAP factors and its corresponding levels. The tolerance for the HSB thickness, TIM thickness, and chip thickness are ± 1, ± 0.002, and ± 0.104 respectively. After running the central composite design (CCD), a fifteen (15) run order were generated for the factors and levels as seen in Table 2. The response for the simulation design is thermal resistance in K/W. Thermal resistance is chosen as the response for this study because it is a vital parameter in the effective conduction of heat in microelectronics packages.

2.2 Materials

The materials used in this work are aluminium, silicon, and lead-free solder (SAC405 having a composition of Sn95.5Ag4.0Cu0.5). SAC405 is used as the material for the TIM because Ekpu *et al* [17] suggested in their work, that SAC405 is a better TIM compared to SAC105 and SAC305. The heat sink is aluminium, the chip is silicon, and the TIM is SAC405. The thermal conductivity of the materials as reported by Ekpu *et al* [18] were 237.5 W/mK, 148 W/mK, and 62 W/mK for aluminium, silicon, and SAC405 respectively.

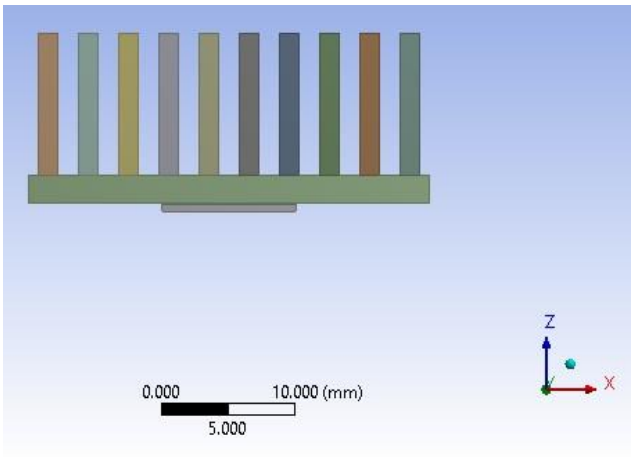

Figure 1: Schematic of a Microelectronic Assembly Package

Table 1: Microelectronics Assembly Package Factors and its Levels

Factors	Unit	Coded Level Low (-)	Coded Level High (+)
Heat Sink Base Thickness	mm	2	5
TIM Thickness	mm	0.035	0.045
Chip Thickness	mm	0.5	1

Table 2: Central Composite Design without Response Data

Run No.	Space Type	Heat Sink Base Thickness (mm)	TIM Thickness (mm)	Chip Thickness (mm)
1	Factorial	2	0.035	0.5
2	Axial	3.5	0.04	1.104
3	Center	3.5	0.04	0.75
4	Factorial	5	0.035	1
5	Center	3.5	0.04	0.75
6	Axial	3.5	0.047	0.75
7	Factorial	2	0.045	1
8	Center	3.5	0.04	0.75
9	Axial	1.379	0.04	0.75
10	Center	3.5	0.04	0.75
11	Axial	3.5	0.033	0.75
12	Center	3.5	0.04	0.75
13	Axial	5.621	0.04	0.75
14	Axial	3.5	0.04	0.396
15	Factorial	5	0.045	0.5

2.3 Load and Boundary Conditions

This investigation adopted steady state thermal analysis based on the temperature dependent parameters shown in Equation 2.

$$\frac{d}{dx}\left(K\frac{dT}{dx}\right)+\frac{d}{dy}\left(K\frac{dT}{dy}\right)+\frac{d}{dz}\left(K\frac{dT}{dz}\right)=0 \qquad (2)$$

Where K is the thermal conductivity, $\frac{dT}{dx}$, $\frac{dT}{dy}$, and $\frac{dT}{dz}$, are the temperature gradients. A heat flow of 5 W was applied to the flip chip, and a natural convection coefficient (5 W/m^{2}K) for stagnant air simplified case was applied on the heat sink. The ambient temperature used for the simulation was 22 ^{o}C and the heat transfer due to radiation was neglected. In this study, it is assumed that heat transfer through conduction starts from the chip through the bonded interface to the heat sink.

3. RESULTS AND DISCUSSIONS

The results from this investigation are presented in Sections 3.1 – 3.7.

3.1 Mesh Analysis

The model used in this investigation was adequately meshed with 92334 nodes and 17813 elements. A mesh dependency study was conducted by Ekpu [19]. In the study, it was concluded that a mesh size between 20% and 40% of the initial size of a model is ideal for having effective results in simulation work done in ANSYS. It is important to note that the mesh result of the present model adhere to the principle presented in [19]. Figure 2 shows the meshed results used in this investigation.

3.2 Temperature and Thermal Resistance Analysis

Temperature output was used as the simulation result because steady state thermal analysis was considered. Figure 3 presents the temperature contour plot of the analysis. By visual inspection of the temperature distribution in Figure 3, it is observed that temperature contours are concentric in nature. Similar temperature contour plots were recorded in Mendonca *et al* [20]. This means that the heat generated by the chip is conducted through the bodies in contact to the surroundings. Maximum temperature could be seen around the chip in Figure 3 with a value of 127.96 ^{o}C, while the minimum temperature of 126.11 ^{o}C occurred on the heat sink. These temperatures were used to calculate the thermal resistances after a parametric analysis were conducted on the different factors and levels of this study. Thermal resistance is given as:

$$R=\frac{\Delta T}{Q} \qquad (3)$$

$$\Delta T = T_{max} - T_{min} \qquad (4)$$

Where Q is the heat flow applied, ΔT is the temperature change in the microelectronics assembly package. The thermal resistance calculated for the different factors and levels were used as the responses of the CCD shown in Table 3.

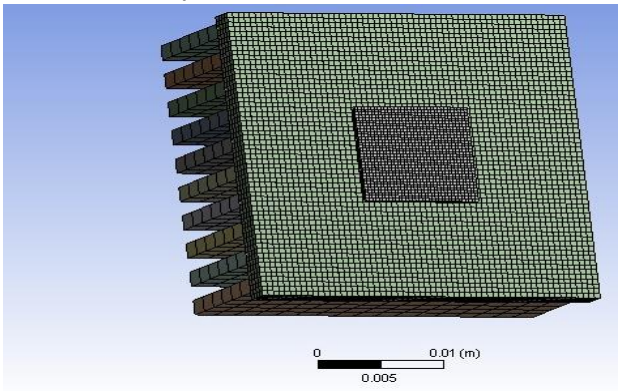

Figure 2: Mesh with 92334 Nodes and 17813 Elements

Table 3: Central Composite Design with Response

Run No.	Space Type	Heat Sink Base Thickness (mm)	TIM Thickness (mm)	Chip Thickness (mm)	Response: Thermal Resistance (K/W)
1	Factorial	2	0.035	0.5	0.37
2	Axial	3.5	0.04	1.104	0.328
3	Center	3.5	0.04	0.75	0.31
4	Factorial	5	0.035	1	0.3
5	Center	3.5	0.04	0.75	0.31
6	Axial	3.5	0.047	0.75	0.31
7	Factorial	2	0.045	1	0.39
8	Center	3.5	0.04	0.75	0.31
9	Axial	1.379	0.04	0.75	0.448
10	Center	3.5	0.04	0.75	0.31
11	Axial	3.5	0.033	0.75	0.31
12	Center	3.5	0.04	0.75	0.31
13	Axial	5.621	0.04	0.75	0.28
14	Axial	3.5	0.04	0.396	0.292
15	Factorial	5	0.045	0.5	0.274

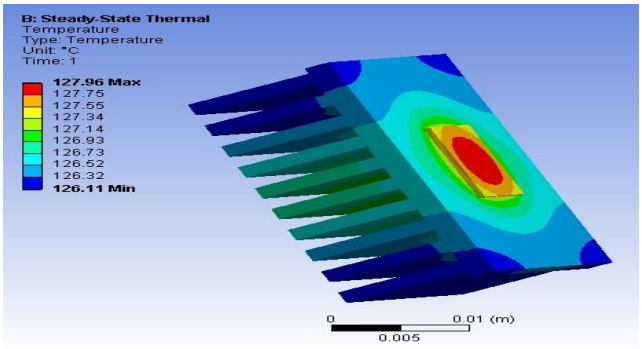

Figure 3: Temperature Distribution Contour Plot

3.3 Analysis of Variance (ANOVA)

The main determining factors in ANOVA are the F-value and p-value. Sada [21], described F-value as the variance of the group means, while p-value is the probability of getting a result at the extreme. Table 4 presents the ANOVA analysis for the quadratic model (thermal resistance). As presented in Table 4, the model has an F-value of 895.40, which implies that the model is significant to the study. According to the ANOVA analysis of Design Expert, there is 0.01% chance that an F-value of 895.40 could happen due to noise. The p-values of the model is 0.0001, meaning it is less than 0.05 thereby indicating that the terms of the model is significant as well. While p-values greater than 0.1 are considered not significant. From Table 4, it could be seen that the significant model terms are A, C, BC, and A^2. Where A is the heat sink base thickness, C is the chip thickness, and B is the TIM thickness.

The goodness of fit statistics validating the thermal resistance response is presented in Table 5. From Table 5, it could be seen that the Predicted R^2 is 0.9330 (93.30%) and the Adjusted R^2 is 0.9983 (99.83%). This demonstrates that over 93.30% of the total variations in the response model could be explained. The difference between both R^2 is about 0.0653 (6.53%) which is less than 0.2 (20%), indicating a reasonable agreement between the Predicted R^2 and Adjusted R^2. The signal-to-noise ratio is measured by Adequate (Adeq) Precision. A signal-to-noise ratio higher than 4 is acceptable in most design analysis [21]. In this study, the signal-to-noise ratio is 110.19, which signifies an adequate signal. This means that the model could be used to navigate the design space.

3.4 Final Equation in Terms of Actual Factors

The final equation in terms of the actual coded factors for the thermal resistance response is presented in Table 6. From Table 6, it is observed that the equation comprises of individual factors and combined factors. The predictions of the thermal resistances for different given levels of each factor could be estimated by the given equation in Table 6 in terms of the actual factors.

It is important to note that the equation in Table 6, is not suitable for determining the relative impact of each factor. This is due to the fact that the coefficients were scaled to address the units of each factor and the intercept is not at the centre of the design space.

3.5 Analysis of Predicted and Actual Responses

The plot of thermal resistance for the predicted and actual values as against the run order is presented in Figure 4. It is observed from Figure 4 that the trend between the predicted values and the actual values are very closely related. This is as a result of the 6.53% difference between both Predicted R^2 (93.30%) and the Adjusted R^2 (99.83%) as discussed in Section 3.3.

In Figure 5, the predicted thermal resistance response is plotted against the actual thermal resistance response. From Figure 5, a linear relationship between the predicted values and actual values could be established. This linear relationship supports the observations from the results discussed in previous sections.

Table 4: ANOVA for Quadratic Model (Thermal Resistance)

Source	Sum of Squares	df	Mean Square	F-value	p-value	
Model	0.0292	9	0.0032	895.40	< 0.0001	significant
A-Heat Sink Base Thickness	0.0141	1	0.0141	3888.00	< 0.0001	
B-TIM Thickness	0.0000	1	0.0000	0.0000	1.0000	
C-Chip Thickness	0.0006	1	0.0006	178.53	< 0.0001	
AB	3.016E-06	1	3.016E-06	0.8308	0.4038	
AC	4.500E-06	1	4.500E-06	1.24	0.3162	
BC	0.0003	1	0.0003	91.65	0.0002	
A^2	0.0053	1	0.0053	1447.00	< 0.0001	
B^2	6.352E-06	1	6.352E-06	1.75	0.2431	
C^2	6.352E-06	1	6.352E-06	1.75	0.2431	
Residual	0.0000	5	3.630E-06			
Lack of Fit	0.0000	1	0.0000			
Pure Error	0.0000	4	0.0000			
Cor Total	0.0293	14				

Table 5: Goodness of Fit Statistics Validating Response

Name	Value	Name	Value
Std. Dev.	0.0019	R^2	0.9994
Mean	0.3235	Adjusted R^2	0.9983
C.V. %	0.5890	Predicted R^2	0.9330
		Adeq Precision	110.1905

Table 6: Final Equation in Terms of Actual Factors

Coefficient Value	Factors
Thermal Resistance	=
+0.210641	
-0.130324	*Heat Sink Base Thickness
+10.06886	*TIM Thickness
+0.471392	*Chip Thickness
+0.163723	*Heat Sink Base Thickness * TIM Thickness
+0.004000	*Heat Sink Base Thickness * Chip Thickness
-10.31758	*TIM Thickness * Chip Thickness
+0.011597	*Heat Sink Base Thickness²
-36.29630	*TIM Thickness²
-0.014519	*Chip Thickness²

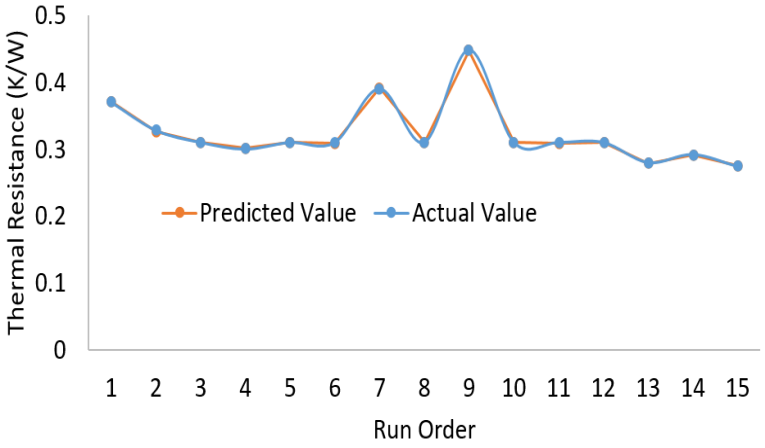

Figure 4: Plot of Thermal Resistance against Simulation Run Order

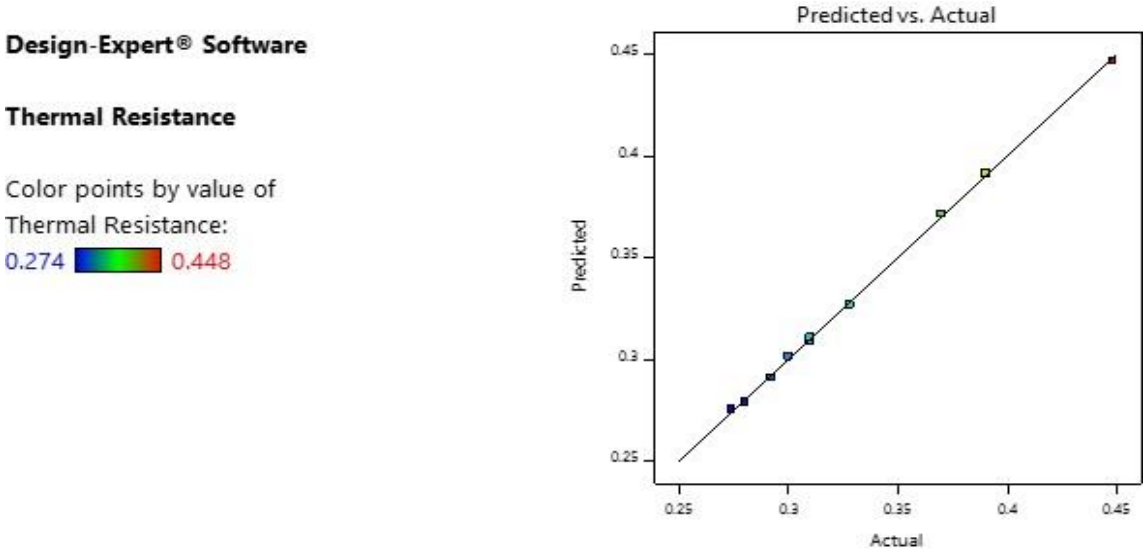

Figure 5: Plot of Predicted vs Actual Thermal Resistance

3.6 Interactions between Factors in Response Surface Methodology (RSM)

The interaction between HSB thickness and TIM thickness at chip thickness of 0.75 mm is presented in Figure 6. The interaction between both factors showed that the thermal resistance is increased when the HSB thickness reduces and the TIM thickness increases. This may be attributed to the differences between both factors interacting. Therefore, having an optimal value for both factors are desired in reducing the thermal resistance. Note that this interaction is at a constant chip thickness.

Figure 7 presents the interaction between HSB thickness and chip thickness at a TIM thickness of 0.04 mm. By visual analysis of Figure 7, it is clearly seen that the thermal resistance is reduced when the chip thickness is low and the HSB thickness is high. Again, this could be attributed to the difference in the thickness of both interacting factors at a constant TIM thickness. Figure 7, also showed that an optimal thermal resistance at 0.04 TIM thickness could be achieved with low chip thickness and high HSB thickness after some trade-off considerations.

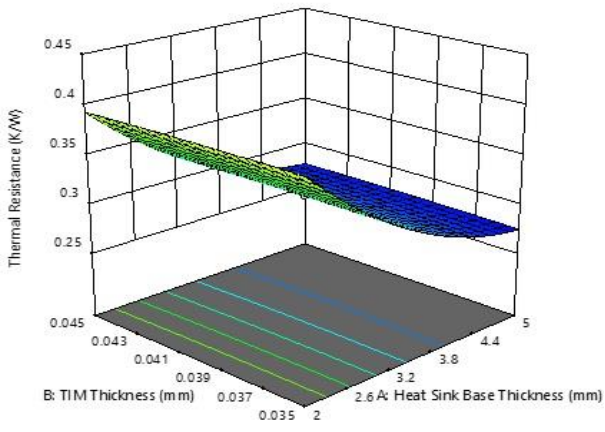

Figure 6: RSM Interaction between HSB Thickness and TIM Thickness

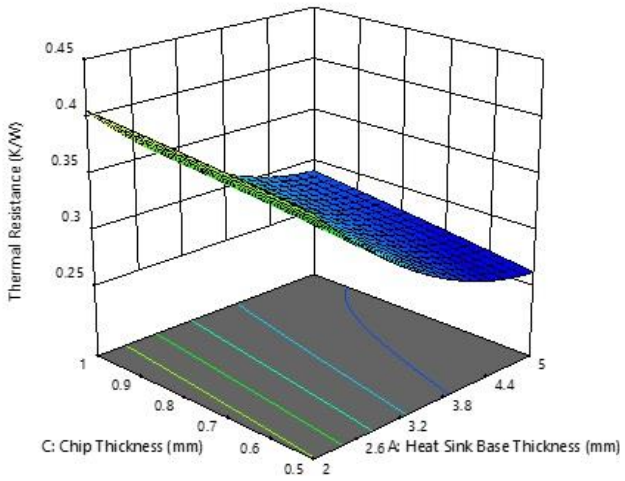

Figure 7: RSM Interaction between HSB Thickness and Chip Thickness

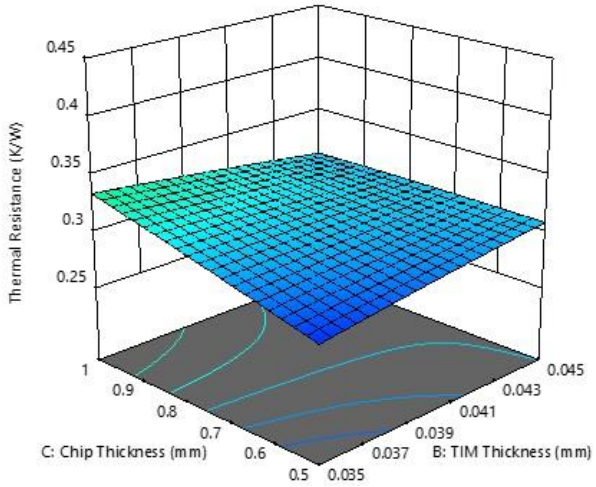

Figure 8: RSM Interaction between TIM Thickness and Chip Thickness

The interaction between TIM thickness and chip thickness at an HSB thickness of 3.5 mm is presented in Figure 8. It is observed from Figure 8, that the thermal resistance from the interaction of both factors are almost the same. This is expected because of the very small thicknesses of both factors considered. From Figure 8, it is seen that thermal resistance is low when the TIM thickness and chip thickness are low. This signifies that there is an effective heat conduction between TIM thickness and chip thickness based on the results of this investigation.

3.7 Optimisation Analysis

This study aimed at having optimal factors that will ensure heat is conducted properly in a microelectronic assembly package, keeping in mind the need to minimise size of the package. From the results discussed in Sections 3.2 – 3.6, it is clearly seen that in order to have an optimal setting for this study the thermal resistance will need to be minimised. From the RSM analyses, the optimal coded level for factors used in this study were given as 3.5 mm, 0.04 mm, and 0.75 mm for HSB thickness, TIM thickness, and chip thickness respectively. The optimal mean thermal resistance based on the optimal factors parameter is given as 0.31052 K/W.

4. CONCLUSIONS

The management of heat in microelectronic devices are necessary for the effective function of the devices. However, getting the right balance in microelectronics assembly package remains crucial for the package performance. Hence, this study have proposed an optimal level combination by using RSM based on the three (HSB thickness, TIM thickness, and chip thickness) components studied. The study concludes that 3.5 mm, 0.04 mm, and 0.75 mm, for HSB thickness, TIM thickness, and chip thickness respectively will give the optimal mean thermal resistance of 0.31052 K/W.

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