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CASCADED SINGLE-PHASE, PWM MULTILEVEL INVERTER WITH BOOSTED OUTPUT VOLTAGE

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ABSTRACT
Splitting of a dc voltage source with two capacitors has been the approach in generating 5-level output voltage with single- and three-phase full-bridge circuits and added bidirectional switch. Associated with this configuration is the problem of voltage imbalance between the splitting capacitors. In addition, the inverter output voltage magnitude is obviously limited to the value of the split input voltage source. Presented in this paper is a unit topology for single-phase 5-level multilevel inverter, MLI. It simply consists of a full-bridge circuit, a capacitor, charge-discharge unit and a dc source. The charge-discharge unit with the capacitor is the interface between the full-bridge and the dc source. The proposed unit cell can generate a 5-level output voltage waveform whose peak value is twice the input voltage value. For higher output voltage level, a cascaded structure of the developed unit cell is presented. Comparing the proposed inverter with CHB inverter and some recent developed MLI topologies, it is found that the proposed inverter configuration generates higher output voltage value, at reduced component-count, than other topologies, for a specified number of dc input voltages. For two cascaded modules, simulation and experimental verifications are carried out on the proposed inverter topology for an R-L load.

Keywords: *Cascaded multilevel, Inverter, total harmonic distortion, topologies, waveform*

1. INTRODUCTION

The emergence and evolution of multilevel inverters (MLIs) have shown significant potential in power electronics applications [1]. Attributed to their competency in reducing output harmonics and transformer-less boosted output voltage, there is a rapidly growing trend of using MLIs for renewable energy integration [2, 3]. The MLI topologies such as neutral point clamped (NPC) [4–7], flying capacitor (FC) [8], and cascaded H-bridge (CHB) [9–12], are the traditional established MLIs which have been extensively researched for electrical energy conversion systems [13, 14].

Findings from the exhaustive researches on these classical multilevel inverter configurations show that they have inherent associated drawbacks. In cascaded H-bridge configuration, multiple isolated voltage sources are required, and for an increased number of output voltage levels, number of power switches increase significantly, [10–12]. Moreover, both in neutral-point-clamped and capacitor-clamped inverters, the problem of voltage balancing, among dc-link series capacitor banks exist, [15–17].

Amongst these fundamental inverter topologies, CHB is a dominant topology for renewable energy conversion systems in view of its voltage boosting capability and modularity. Recently, the research trend is steered towards the modification of the H-bridge by module configurations with higher compactness and less switch count. The developed module topologies are able to generate more voltage levels while at the same time offer higher efficiency [18, 19]. The switched DC sources concept from CHB is mostly retained as it remains a popular approach in generating multiple voltage levels [20]. The principal concept of module topology generally involves the insertion of extra circuitry to produce more voltage level across DC link of H-bridge. Such extra circuitry in most cases has an independent voltage sources and/or switched capacitor banks. Such improvement

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will facilitate the separate control of voltage level generation and output voltage steering. Works presented in [21–28] are some the recent inverter topologies, with their corresponding control strategies, which utilizes the aforementioned principle. In all, the focus is to obtain appreciable high level of pre-stepped output voltage waveform which is impressed on an H-bridge for onward voltage inversion.

In [21], the module configuration is a cascade of half-bridge circuits with individual isolated dc sources. Therein, a cascade of six half-bridge cells was demonstrated; resulting in a 13-level single-phase output voltage waveform. Similar power circuits were presented in [22 – 25]. The bane of these configurations is the isolated dc source demand for each output voltage step. This issue was alleviated in the works done in [26] and [27], wherein switched capacitor banks were employed in the module configuration. In [27], less number of circuit-component-count was achieved both in the symmetrical and asymmetrical configurations when compared to the power circuit in [26]. In both configurations, the capacitor voltage values need to be controlled; involving extra control circuit.

Use of bidirectional switch to link a cascade of two dc sources to the H-bridge was proposed by Sung-Jun Park and others, [28]. This single-phase inverter configuration synthesises 5-level output voltage waveform per cycle; and hence exhibits a better performance than the 3-level H-bridge with respect to total harmonic distortion (THD) value. For higher output voltage level, work done in [29] extended this topology to accommodate more dc sources. In view of three-phase applications, Jafferi Jamaludin extended the work in [29] to three-phase system, [30]. Therein, the bidirectional switches' usage was optimized following a space vector modulation control approach. In [28 – 30], it is apparent that the demand for isolated dc sources is inherently needed in these topologies. The provision of these isolated supplies is the main limitation in the power electronic circuit design.

In [31], the two isolated dc sources in [28] were replaced with two capacitor banks, which split a single dc voltage source; the configuration is shown in Fig. 1(a). The power circuit switch-count and operational principle remain same. A single-phase cascaded structure of this capacitor-split single input, 5-level inverter configuration was presented in [32]; wherein a configuration for 9-level output voltage waveform synthesis was demonstrated. The work done in [33] extended the cascaded configuration in [32] to three-phase system. Focusing still on three-phase system, the H-bridge in [28] was replaced with 3-phase Bridge in [34] and [35]; therein, 5- and 7-level, line-line output voltage waveforms were generated, respectively. The inverter topology proposed in [31] has an output voltage magnitude limitation; dictated by the sole dc input source. Besides, there is voltage imbalance between the splitting capacitor banks; and this necessitates additional control circuit in this inverter configuration, as well as its derivatives in [32 – 35].

Under these technical backgrounds, this paper presents a cascaded single-phase, PWM multilevel inverter topology with capacitor-boosted output voltage. The proposed basic unit for the cascaded structure proffers solutions to the problem inherent in [28] and [31]. Hence the basic unit, with a single dc input, is capable of synthesizing 5-level output voltage waveform; whose amplitude is twice the input voltage value. Moreover, only one capacitor bank is used; therefore, the issue of voltage imbalance does not arise. The proposed cascaded multilevel inverter circuit is very much similar to the CHB inverter configuration. The difference is that in each H-bridge cell, a capacitor and its charge–discharge circuit has been added to boost the output voltage and as well improve the overall harmonic profile of the output waveforms. Also, the proposed cascaded inverter structure operationally resembles that presented in [32] with regards to the output voltage waveform and its spectrum. However, the distinct difference and hence the improvement is apparently seen on the boosted output voltage value and absence of splitting capacitor banks; with their associated imbalance problem. Moreover, the component-count of the proposed inverter configuration is highly reduced when compared with the conventional CHB inverter; and is at par with configuration in [32] for the same output voltage level. Operational principles and switching functions are analysed. Simulation and experimental results are presented to verify the validity of the proposed inverter.

2. OPERATIONAL PRINCIPLES

Beginning with the basic unit configuration, the switching sequence/pattern that result in the output voltage level syntheses are discussed in this section. The generalized cascade structure of the basic unit is

presented. Also, the modulation scheme for each unit as well as for the cascaded configuration is given.

2.1 Circuit configuration and operation

Shown in Fig. 1(b) is the power circuit of a unit cell/module of the proposed cascaded multilevel inverter configuration.

This module comprises of an H-bridge, a capacitor bank, simplified charge–discharge circuit and a dc source. The charge-discharge unit, with the capacitor bank, interfaces the H–bridge to the dc source. The charge-discharge unit is made up of two active switches and a diode;

one of the switches has no free-wheeling diode. This ensures a unidirectional discharge of the capacitor bank. The two switches are connected in a half-bridge fashion whose output node links the capacitor bank. The diode connects the capacitor bank and the negative rail of the H-bridge to the negative terminal of the input voltage source; this node is also shared by the negative rail of the half-bridge. The positive rails of the half- and H-bridges and the input voltage source are linked together.

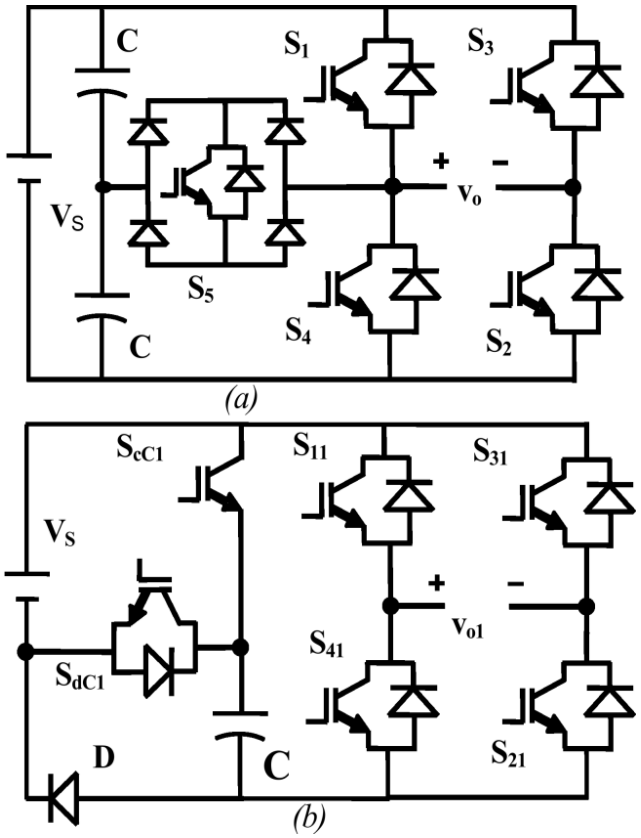


Fig. 1. *Single-phase 5-level inverter configurations. (a) Inverter configuration presented in [31] (b) proposed inverter module*

With this circuit components arrangement, proper control of the switches in the H-bridge and the charge–discharge circuit in this inverter unit can produce 5 output voltage levels: 0, V_s, $2V_s$, $-V_s$, and $-2V_s$. Considering the positive half cycle of the synthesized output voltage, v_{o1}, the basic operational modes are shown in Figures 2(b) – (d).

The switching states of the power switches and the corresponding synthesized output voltages are summarized in Table 1. With this described inverter module, Fig. 3 shows the generalized cascaded structure of the proposed inverter topology.

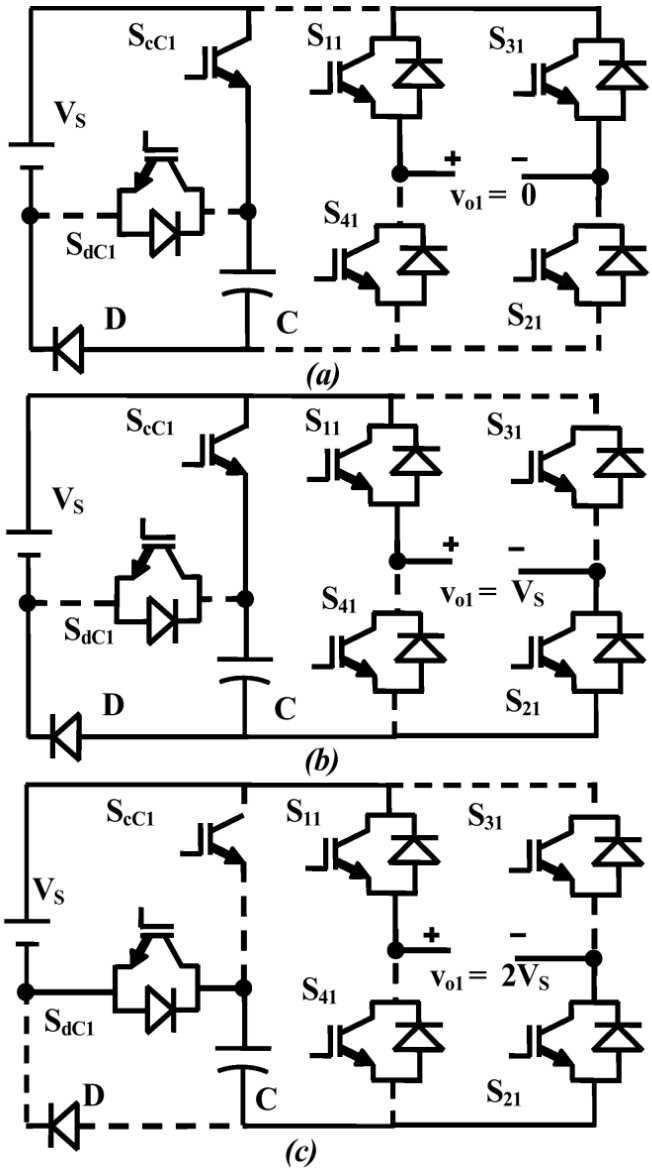


Fig. 2. *Proposed inverter module operational modes.*

2.2 Modulation scheme

The modular structure of the power circuit in figure 3 is an indication that the modulation/control of the cascaded units should follow suit. Hence, in each of the cascaded units, single carrier sinusoidal pulse-width modulation

(SCSPWM) scheme is employed in the generation of the six gating signals. The principle of the switching strategy is to generate gating signals by comparing rectified sinusoidal modulating/reference signals, at the fundamental frequency, with only one triangular carrier at the desired switching frequency; whose peak-to-peak amplitude is A_c. For *n*-level SCSPWM, *k* number of rectified sinusoidal modulating signals have the same fundamental frequency, f_m, and amplitude, A_m, with dc bias of A_c as a difference between these signals, [36–38]. The switching/modulation scheme adopted in each of the cascaded inverter cells is illustrated in Fig. 4.

From this Fig. 4, if the sine signal, *R*, is compared to the zero value, switching signal S_{11} is generated. Also, comparing the carrier signal, *T*, with the voltage references, R_1 and R_2, the rest of the switching signals are then given by the use of basic logical AND, OR, NOT gates.

$$S_{11} = R > 0 \quad (1)$$

$$S_{31} = \{ [(T > R_1) \bullet S_{11}] + [(\overline{T > R_1}) \bullet \overline{S_{11}}] \} \quad (2)$$

$$S_{cC1} = T > R_2 \quad (3)$$

S_{41}, S_{21}, and S_{dC1} gating signals are obtained by negating S_{11}, S_{31}, and S_{cC1}, respectively.

In order to cascade several *N* modules effectively, the carrier signals of *N*-different inverter cells are shifted by (360/*N*)° sequentially from one another, so that the cascaded inverter cells can generate 4*N*+1 level output voltage. In this work, two modules are cascaded and the carrier signals are shifted by 180° from each other in order to generate 9-level output voltage waveform at the load terminals, as shown in Fig. 5.

In each of the cascaded inverter cells, the frequency and amplitude modulation indices expressions are given as

$$M_f = \frac{f_c}{f_m} \quad (4)$$

$$M_a = \frac{A_m}{A_c(k-1)} \quad (5)$$

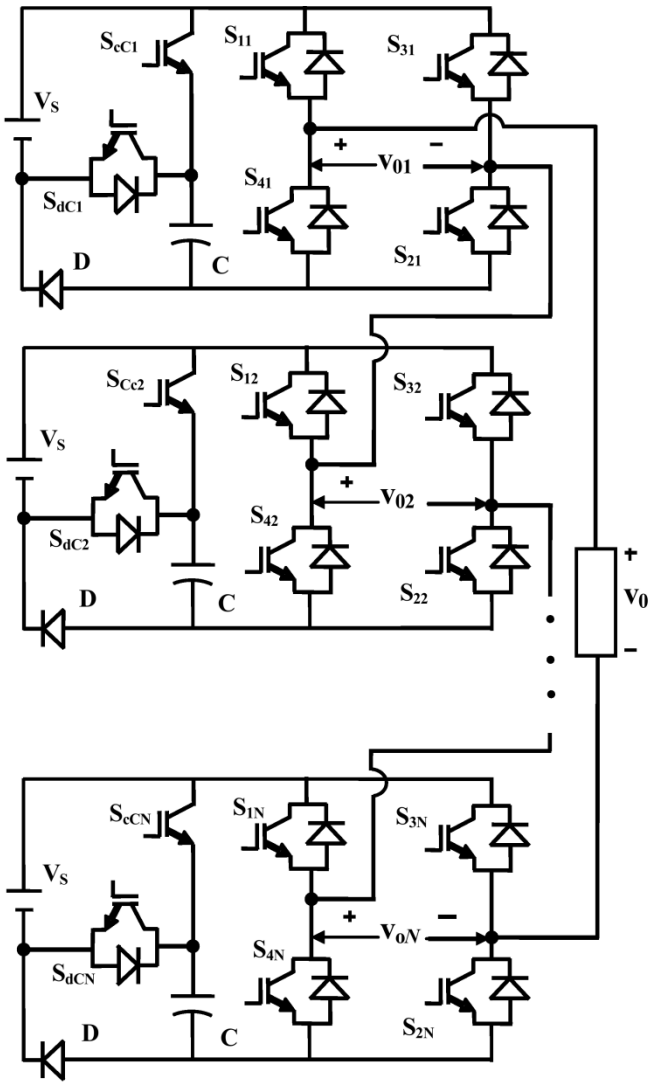


Fig. 3. *Proposed cascaded multilevel inverter*

Table 1 Switching states and the synthesized output voltages of the proposed unit module.

V_{c1}	S_{cC1}	S_{dC1}	S_{11}	S_{21}	S_{31}	S_{41}
0	1	0	1	0	1	0
Vs	1	0	1	1	0	0
2Vs	0	1	1	1	0	0
0	1	0	0	1	0	1
-Vs	1	0	0	0	1	1
-2Vs	1	0	0	0	1	1

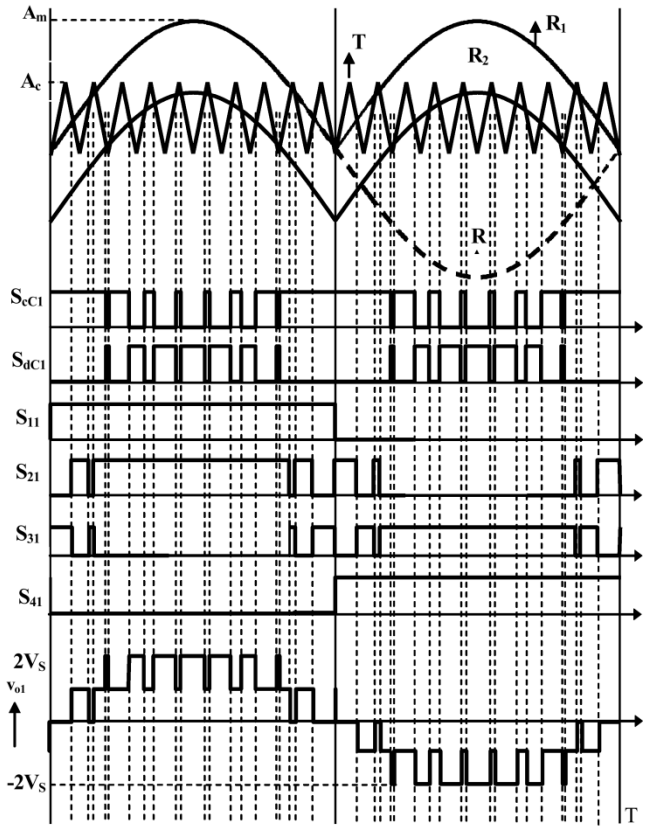


Fig. 4. *Single-carrier sinusoidal PWM switching scheme for a module in the proposed cascade multilevel inverter configuration.*

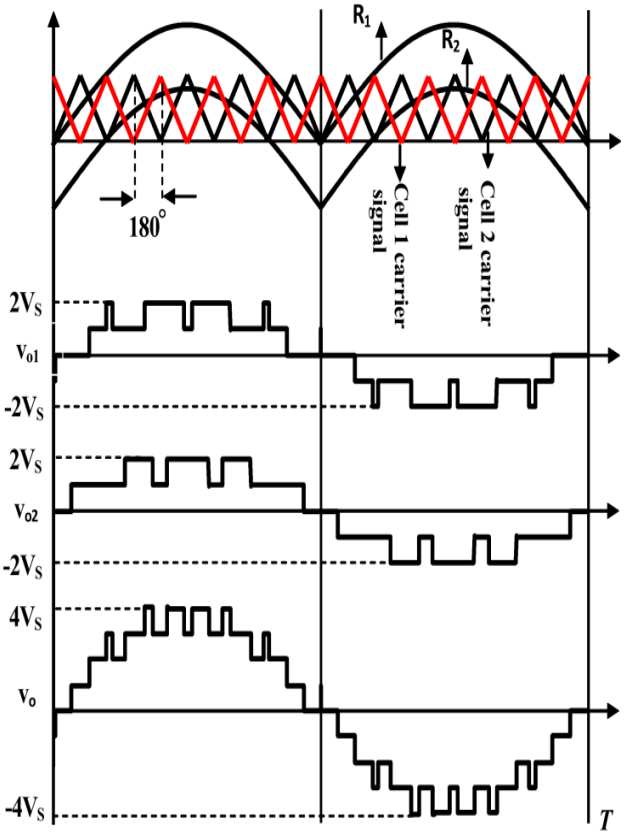


Fig. 5. *Cascading two modules of the proposed MLI*

Where f_c and f_m are the frequencies of the triangular carrier and modulating signals, respectively. A_c and A_m are the corresponding peak-to-peak values of the signals, as shown in figure 4. *k* is the number of voltage level synthesized per half-cycle; in this case, k = 3.

3. COMPARISON BETWEEN THE PROPOSED INVERTER, CLASSICAL CHB AND SOME RECENT MODULE MLI CONFIGURATIONS

Certain figures of merits are usually considered when assessing the enhancement/improvement in a given MLI configuration. Some of these figures are: number of isolated dc sources, number of synthesized voltage levels, number of active and passive switches, peak inverse voltage, (PIV), of the switches, number of conducting switches (on-state switches) required to synthesize a given voltage level, et cetera. Correspondingly, these figures dictate the size, quality of the output voltage waveform and filtering level, cost and loss dissipation in any given MLI configuration.

The proposed cascaded MLI shown in figure 3 is compared with the classical symmetrical CHB and recent similar symmetrical MLI topologies proposed in [28], [31–33] and [38–41]. The comparison is shown in Table 2 based on the aforementioned criteria, for a given number, *x*, of the input dc voltage source, V_S. Assessment of Table 2 shows that for the same number of dc input voltage, the proposed module inverter increases both the number of level and magnitude of output voltage by 50% when compared to the classical CHB inverter module; at the expense of additional two active switches. As commented earlier in the introductory section, inverter configuration in [31] and its derivatives need large value of two splitting-capacitor banks to prevent asymmetry of dc-link voltages. The number of needed capacitor banks has been reduced by 50% in the proposed inverter module and the issue of asymmetry arises not thereof. Moreover, the output voltage receives a boost of 50% in magnitude in the proposed configuration when compared to the topologies in [28], [31–33] and [40]. As seen from Table 2, the most outstanding advantage of the proposed inverter is the reduced number of input voltage source and the output voltage boost.

4. LOSS CALCULATION

The dominant and prominent losses associated with semiconductor power switches in pulse width

modulated power electronics circuits are conduction and switching losses. The former loss are caused by the equivalent resistance and the inherent on-state voltage drop of the semiconductor devices; whilst the latter loss are caused by non-ideal switching of the devices, manifested as the power dissipation during turn-on and turn-off switching transitions. Analytical derived expressions for the conduction power losses in semiconductor switches can be obtained in terms of the modulation index, M_a, power factor, ϕ, and output parameters: voltage and current amplitudes, for typical conditions present in PWM inverters, [42]. For each of the IGBTs and diodes used in Fig. 3, good estimations for their average on-state losses, L_{con_SW} and L_{con_SW} were:

$$L_{con\_SW} = \left[\begin{array}{l} \frac{V_{SWon} I_m}{2\pi} \left\{ 1 - \frac{\pi}{4} M_a \cos\phi \right\} \\ + \frac{R_{SWon} {I_m}^2}{2\pi} \left\{ \frac{\pi}{4} - \frac{2}{3} M_a \cos\phi \right\} \end{array} \right] \quad (6)$$

$$L_{con\_D} = \left[\begin{array}{l} \frac{V_{Don} I_m}{2\pi} \left\{ 1 - \frac{\pi}{4} M_a \cos\phi \right\} \\ + \frac{R_{Don} {I_m}^2}{2\pi} \left\{ \frac{\pi}{4} - \frac{2}{3} M_a \cos\phi \right\} \end{array} \right] \quad (7)$$

where V_{SWon}, V_{Don} are the constant on-state voltages across a switch and diode; R_{SWon}, R_{Don} are the on-state resistances, respectively; I_m, M_a *and* ϕ are the peak load current through a device, modulation index and power factor angle, respectively. The first terms in (6) and (7) are the losses due to the constant components of on-state voltage V_{SWon} *and* V_{Don}; while the second terms are the losses due to the linear dependence on current of the on-state voltages as expressed in terms of R_{SWon} *and* R_{Don}. Hence, the overall conduction loss is

$$L_{con} = L_{con\_SW} + L_{con\_D} \quad (8)$$

During switching transitions in power semiconductor devices, switching losses, L_{SW}, are generated; and are directly proportional to the switching frequency, f_C. During one reference period, the switching loss for every power device is obtained by identifying every turn-on and turn-off instants, θ. Present in the manufacturer's datasheets are the characteristic curves of each power device. The semiconductor average switching losses can be estimated from these characteristic curves. The IGBT model used in the laboratory prototype of the proposed inverter configuration is GW40N120KD.

Table 2 Comparison of between the proposed inverter, classical symmetrical CHB and some recent cascaded symmetrical MLI topologies proposed.

Topologies	Number of dc sources, *x*.	Number of capacitor bank	Number of active switches	Number of diodes	Number of output voltage level	Maximum voltage generated	Peak inverse voltage (PIV)	On-state switches
CHB	*x*	*0*	*4x*	*0*	*2x+1*	xV_S	xV_S	*2x*
Circuit in [28]	*x*	*0*	*5x*	*4x*	*4x+1*	xV_S	xV_S	*3x*
Circuit in [31–33]	*x*	*2x*	*5x*	*4x*	*4x +1*	xV_S	xV_S	*3x*
Circuit in [38–39]	2*x*	*0*	*6x*	*0*	*4x +1*	$2xV_S$	$2xV_S$	$\frac{3x}{2}$
Circuit in [40]	*x*	*2x*	*3x*	*4x*	*2x +1*	xV_S	$\frac{xV_S}{2}$	*3x*
Circuit in [41]	*x*	*2x*	*10x*	*0*	*8x+1*	$2xV_S$	$2xV_S$	*2x*
Proposed								

Considering its switching loss, the characteristics curves which represent the energy losses during commutation are: turn-on commutation loss, $E_{on}(\theta)$, turn-off commutation loss, $E_{off}(\theta)$, and diode recovery commutation loss, $E_{rec}(\theta)$. These curves are approximated by exponential equations, using curve-fitting tool in MATLAB. Mathematical models obtained for the IGBTs, and are given as:

$$E_{on} = \begin{bmatrix} 0.0041e^{0.0044 M_a I_m \sin(\theta-\phi)} \\ -0.0037e^{-0.0088 M_a I_m \sin(\theta-\phi)} \end{bmatrix} \quad (9)$$

$$E_{off} = \begin{bmatrix} 0.00443e^{0.0021 M_a I_m \sin(\theta-\phi)} \\ -0.0547e^{-0.00107 M_a I_m \sin(\theta-\phi)} \end{bmatrix} \quad (10)$$

$$E_{rec} = \begin{bmatrix} 0.00806e^{-0.000322 M_a I_m \sin(\theta-\phi)} \\ -0.0077e^{-0.00446 M_a I_m \sin(\theta-\phi)} \end{bmatrix} \quad (11)$$

Hence, the average switching loss is expressed as

$$L_{SW} = \left(\frac{f_C}{2\pi}\right)\left(E_{on} + E_{off} + E_{rec}\right) \quad (12)$$

The total converter loss, P_{loss}, is then

$$L_{loss} = L_{con} + L_{sw} \quad (13)$$

5. SIMULATION AND EXPERIMENTAL RESULTS

Following the earlier discussions in Sections 1 and 2 regarding the operational principles and the modulation scheme for the proposed cascaded MLI, the verification simulation and validating experimental results are presented in this section.

5.1 Simulation results

From figure 3, a cascade of two inverter modules is used to demonstrate the features of the proposed inverter topology; wherein the switching scheme depicted in Figs. 4 and 5 were used. MATLAB Simulink and Plecs simulations were carried out with arbitrary RL load; R and L are 25Ω and 90mH respectively. The carrier/switching frequency is 3kHz. The dc input voltage, V_S, is 150V and the capacitor, C, has a capacitance value of 2500μF. Fig. 6 shows the simulated inverter output voltages and current waveforms for a modulation index of 0.9. The spectral analyses result of this synthesized inverter output waveforms are displayed in Fig. 7. Therein, THD values of 32.01% and 16.21% are achieved in each of the 5-level cascaded modules and overall 9-level output voltage waveforms, respectively.

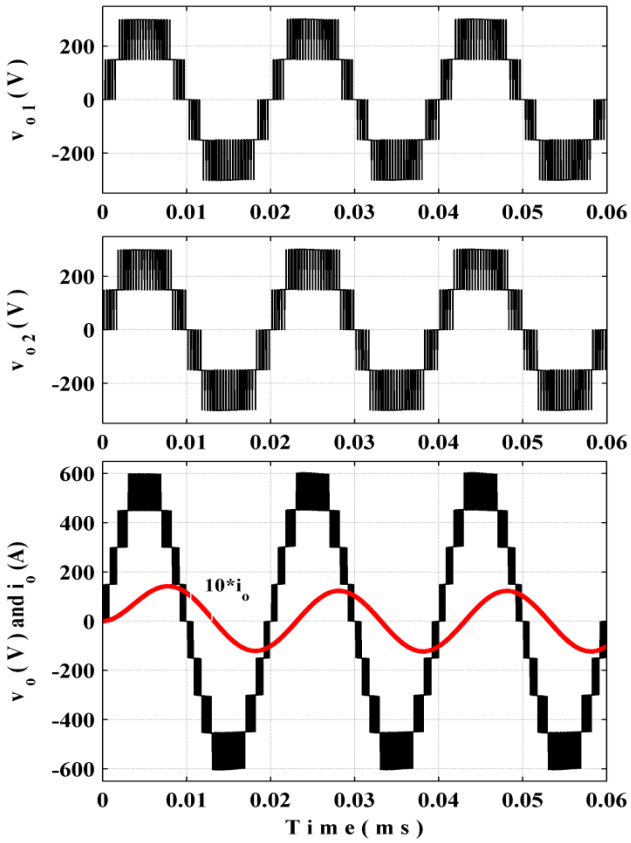


Fig. 6. Simulated inverter output voltages and current waveforms

Table 3 Prototype specification

Power switches: GW40N120KD
Power diodes: DPG30P300PJ
R = 25Ω , L = 90mH
Capacitor, C = 2500μF, 400V
Dc input voltage: V_S= 150V

5.2 Experimental results

In line with the simulation results, a laboratory prototype of the cascaded MLI was built; the prototype specifications and parameters are given in Table 3. The modulation scheme presented in section 2 is implemented in the prototype, resulting in the generation of the 6 gating signals for each of the cascaded modules.

At 0.9 depth of modulation, Fig. 8 shows typical logic gating signals, the experimental waveforms of the inverter output voltages and the corresponding load current for the specified loading condition in Table 3.

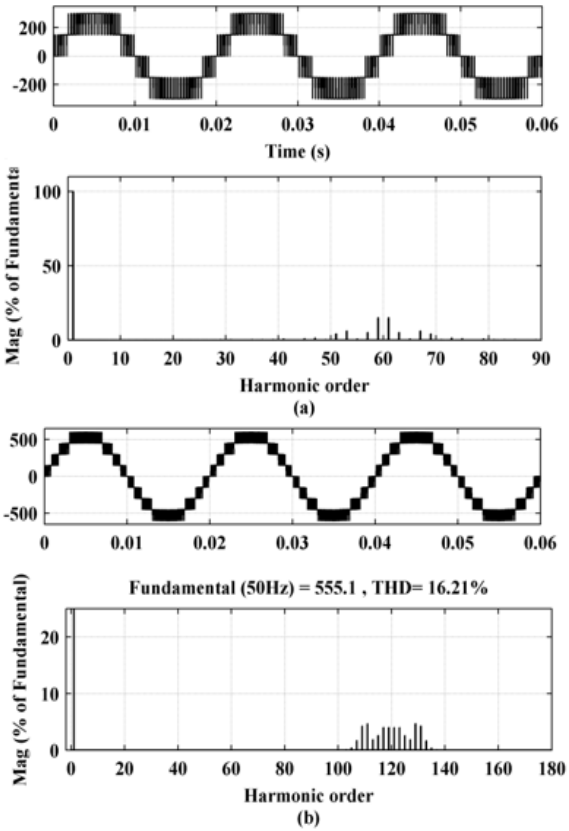
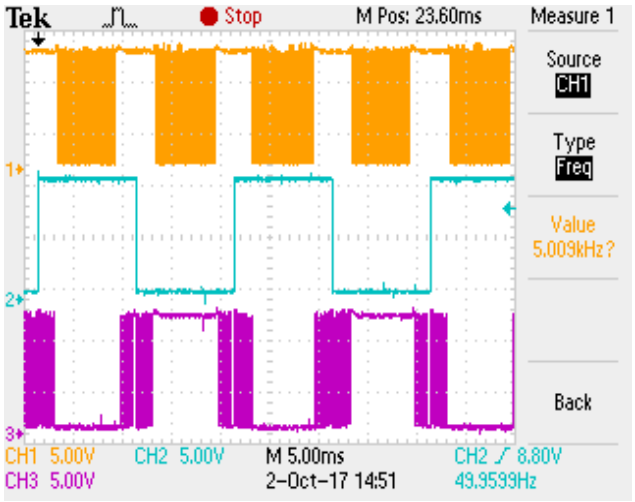


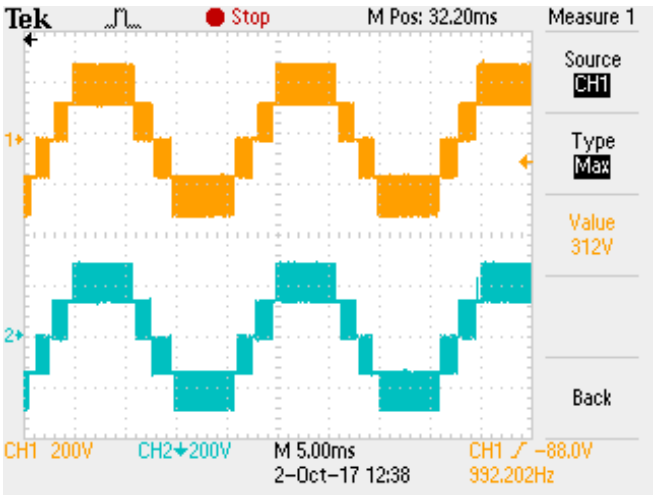
Fig. 7. *FFT analyses of the synthesized inverter output voltages. (a) module voltage waveform spectrum. (b) cascaded output voltage waveform spectrum.*

6. CONCLUSION

In this paper, an enhanced configuration for cascaded multilevel inverter is presented with regards to the unit cells output voltage magnitude and component-count. The switching principles, modulation scheme and switching functions have been given in detail. Out of the six power switches in each unit cell, three switches are simultaneously turned on for the synthesis of any of the output voltage level. Two of these switches are pulse-width modulated while one is switched at the fundamental frequency; this ensures minimum number of switching transitions among the power switches. Each of the modules in the proposed cascaded MLI can synthesize a maximum of 5-level output voltage waveform; whose amplitude is twice that of the single input voltage source. A comparison has been made, with respect to specified figure of merits, between the proposed inverter circuit, classical CHB inverter and some of the recent developed MLI topologies. For two cascaded inverter modules and for typical modulation index of 0.9, the frequency spectra of the synthesized output voltage waveforms of the proposed inverter configuration have been shown. Also, a good approximation for the average power loss in the active and passive power switches is given in simple expressions in terms of current amplitude, depth of modulation and power factor for typical conditions prevailing in PWM inverters. The operation of the proposed inverter topology has been demonstrated through simulations and laboratory experiments on the proposed inverter for an R-L load; results have been adequately presented.



(a)



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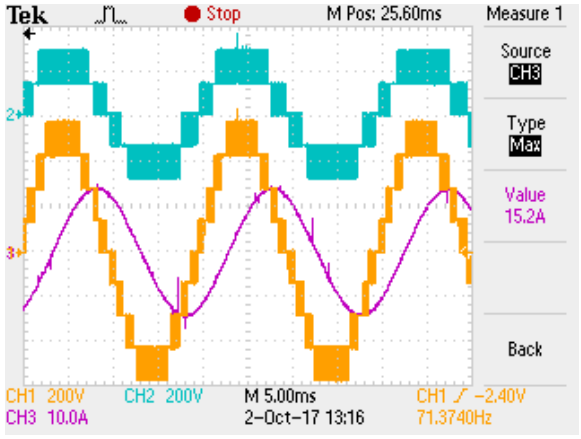

(c)

Fig. 8. Experimental inverter waveforms.
(a) Gating signals S_{cC1}, g_1 and g_3.
(b) module output voltages, v_{o1} and v_{o2}.
(c) module output voltage, v_{o1}, cascaded inverter output voltage, v_o and load

7. ACKNOWLEDGEMENT

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8. REFERENCES

[1] H. Akagi, "Multilevel Converters: Fundamental Circuits and Systems," *Proc. IEEE,* vol. PP, no. 99, 2017.

[2] P. Kala and S. Arora, "A Comprehensive Study of Classical and Hybrid Multilevel Inverter Topologies for Renewable Energy Applications," *Renew. Sustain. Energy Rev.*, vol. 76, pp. 905–931, 2017.

[3] C. Cecati, F. Ciancetta, and P. Siano, "A Multilevel Inverter for Photovoltaic Systems with Fuzzy Logic Control," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4115–4125, 2010.

[4] Baker RH. High-voltage converter circuit. US Patent 04-203- 151; May 1980.

[5] Nabae A, Takahashi I, Akagi H. A new neutral-point clamped PWM inverter. *In: Proceeding of the industry application society conference*; 1980. p. 761–6.

[6] AkiraNabae, Isao Takahashi, and HirofumiAkagi, "A New Neutral-point Clamped PWM inverter," *IEEE Trans. Ind. Applicat.,* vol. IA-17, pp. 518-523, Sept./Oct. 1981.

[7] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[8] Meynard, T. A., and Foch, H., "Multi-level conversion: high-voltage chopper and voltage source inverters," *Conference Record of the 1992 IEEE Power Electronics Specialists Conference (PESC)*, pp. 397–403, Toledo, Spain, 29 June–3 July 1992.

[9] Baker RH. Electric power converter. US Patent 03-867-643; February 1975.

[10] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[11] H. Sepahvand, J. Liao, M. Ferdowsi, and K. A. Corzine, "Capacitor voltage regulation in single-DC-source cascaded H-bridge multilevel converters using phase-shift modulation," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3619–3626, Sep. 2013.

[12] B. P.McGrath, D. G. Holmes, andW. Y. Kong, "A decentralized controller architecture for a cascaded H-bridge multilevel converter," *IEEE Trans.Ind. Electron.*, vol. 61, no. 3, pp. 1169–1178, Mar. 2014.

[13] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters,"*IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, 2010.

[14] J. Rodríguez, Jih-Sheng Lai and Fang Zheng Peng, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, 2002.

[15] G. P. Adam, S. J. Finney, A. M. Massoud, and B.W.Williams, "Capacitor balance issues of the

diode-clamped multilevel inverter operated in a quasi-two-state mode," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 3088– 3099, Aug. 2008.

[16] Z. Shu, N. Ding, J. Chen, H. Zhu, and X. He, "Multilevel SVPWM with DC-link capacitor

voltage balancing control for diode-clamped multilevel converter based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1884–1896, May 2013.

[17] K. Wang, Y. Li, Z. Zheng, and L. Xu, "Voltage balancing and fluctuationsuppression methods of

floating capacitors in a new modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1943–1954, May 2013.

[18] X. Yuan, "Derivation of Voltage Source Multilevel Converter Topologies," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 966–976, 2017.

[19] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel Inverter Topologies with Reduced Device Count: A Review," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 135–151, 2016.

[20] K. K. Gupta and S. Jain, "A Novel Multilevel Inverter Based on Switched DC Sources," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3269–3278, 2014.

[21] Gui-Jia Su, "Multilevel DC-Link Inverter," *IEEE Trans. Ind. Applicat.,* vol. 41, no. 3, pp. 848–854, 2005.

[22] Ehsan Najafi and Abdul Halim Mohamed Yatim, "Design and Implementation of a New Multilevel Inverter Topology," *IEEE Trans. Ind. Electron.*, vol. 59, no. 11, pp. 4148–4154, 2012.

[23] Charles Ikechukwu Odeh, "Cascaded half-full-bridge PWM multilevel inverter configuration," *Turk J Elec Eng & Comp Sci.*, vol. 24, no. 4, pp. 2071–2083, 2016.

[24] Mohammad Farhadi Kangarlu and Ebrahim Babaei, "A Generalized Cascaded Multilevel Inverter Using Series Connection of Sub-Multilevel Inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 625–636, 2013.

[25] Sze Sing Lee, Bing Chu, Nik Rumzi Nik Idris, Hui Hwang Goh, and Yeh En Heng ,"Switched-Battery Boost-Multilevel Inverter with GA Optimized SHEPWM for Standalone Application ," *IEEE Trans. Ind. Electron.,* vol. 63, issue 4, pp. 2133–2142, 2016.

[26] Ebrahim Babaei, "A Cascade Multilevel Converter Topology with Reduced Number of Switches," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2071–2083, 2016.

[27] Javad Ebrahimi , Ebrahim Babaei and Gevorg B. Gharehpetian, "A Cascade Multilevel Converter Topology With Reduced Number of Switches," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 655–667, 2012.

[28] Park, S.-J., Kang, F.-S., Lee, M.H., Cheul-U-Kim: 'A new single-phase, five-level PWM inverter employing a deadbeat control scheme', *IEEE Trans. Power Electron.*, 2003, 18, (3), pp. 831–843

[29] Rasoul Shalchi Alishah, Daryoosh Nazarpour, Seyed Hossein Hosseini and Mehran Sabahi,"Novel multilevel inverter topologies for medium and high-voltage applications with lower values of blocked voltage by switches ," *IET Trans. Power Electron.*, Vol. 7, Iss. 12, pp. 3062–3071, 2014.

[30] Jafferi Jamaludin, Nasrudin Abd. Rahim and Hew Wooi Ping, "Multilevel voltage source inverter with optimised usage of bidirectional switches," *IET Power Electron.*, Vol. 8, Iss. 3, pp. 378–390, 2015.

[31] Nasrudin A. Rahim and Jeyraj Selvaraj," Multistring Five-Level Inverter With Novel PWM Control Scheme for PV Application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2111–2123, 2010.

[32] Charles I. Odeh and Damian B.N. Nnadi, "Single-phase 9-level hybridised cascaded multilevel inverter," *IET Power Electron.*, Vol. 6, Iss. 3, pp. 468–477, 2013.

[33] Nasrudin A. Rahim, Mohamad Fathi Mohamad Elias and Wooi Ping Hew, "Transistor Clamped H-Bridge Based Cascaded Multilevel Inverter with New Method of Capacitor Voltage Balancing," *IEEE Trans. Ind. Electron.,* vol. 60, no. 8, pp. 2943–2956, 2013.

[34] Charles I. Odeh, Damian B. Nnadi and Emeka S. Obe "Three-phase, Five-level Multi-Level Inverter Topology," *Electric Power Components and Systems*, vol. 40, Iss.13, pp. 1522–1532, 2012

[35] Charles Ikechukwu Odeh," Enhanced three-phase multilevel inverter configuration," *IET Power Electron.*, Vol. 6, Iss. 6, pp. 1122–1131, 2013.

[36] M. S. A. Dahidah and V. G. Agelidis, "Single carrier sinusoidal PWM equivalent selective harmonic elimination for a five level voltage

source inverter," *Electr. Power Syst. Res.*, vol. 78, no. 1, pp. 1826–1836, Nov., 2008.

[37] D. Grahame Holmes and Thomas A. Lipo, *Pulse Width Modulation for Power Converters, Principles and Practice.* A John Willey and sons, Inc., Publication, USA, 2003.

[38] Odeh, C. I., "A Cascaded Multi-Level Inverter Topology with Improved Modulation Scheme" *Electric Power Components and Systems*, 42:7, pp. 768–777, 2014.

[39] Ebrahim Babaei, Sara Laali and Somayeh Alilu, "Cascaded Multilevel Inverter with Series Connection of Novel H-Bridge Basic Units," *IEEE Trans. Ind. Electron.,* vol. 61, no. 12, pp. 6664–6671, 2014.

[40] Reza Barzegarkhoo, Elyas Zamiri, Naser Vosoughi, Hossein Madadi Kojabadi and Liuchen Chang, "Cascaded multilevel inverter using series connection of novel capacitor-based units with minimum switch count," *IET Power Electron.*, Vol. 9, Iss. 10, pp. 2060–2075, 2016.

[41] Odeh, C. I. and Vincent N. Agu, "Cascaded Common Nodal Point Multi-Level Inverter Topology" *Electric Power Components and Systems,* 45:7, pp. 534–547, 2017.

[42] L.K. Mestha and P.D. Evans, "Analysis of on-state losses in PWM inverters," *IEE Proceedings,* vol. 136, Pt. B, No. 4, pp. 189 – 195, July 1989.