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OPTIMIZATION OF INSULATED HfO_2 DIELECTRICS OF GaN/InN/GaN/ $In_{0.1}Ga_{0.9}N$ ENHANCEMENT MODE OF MIS-HEMT HETEROSTRUCTURE FOR HIGH FREQUENCY POWER AMPLIFIER APPLICATIONS

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ABSTRACT
In this paper, the enhancement-mode operation of the hetestructure of GaN/InN/GaN/$In_{0.1}Ga_{0.9}N$ of the Metal Insulator Semiconductor High Electron Mobility Transistor (MIS-HEMTs) device having InN-channel was investigated. The effect of scaling the device dimensions of Metal Insulator, such as the dielectric thickness of HfO_2 and the channel lengths, on the electrical performances was analyzed and compared to the currently used heterostructure. The numerical simulation of synopsis TCAD used showed a significant improvement in the electrical properties of the device that achieved a threshold voltage (V_T) = 0.828 maximum drain current of 1.77 A/mm V, transconductance (g_m) of 2.29 S.mm^{-1}, lowest ON-state resistance (R_{ON}) of 0.21 Ω.mm, and along with high-frequency performance achieving f_T/ f_{max} of 98 GHz/129 GHz and 200 GHz/ 360 GHz respectively. The simulations also showed that this scaled GaN/InN/GaN/$In_{0.9}Al_{0.1}N$ heterostructure MIS-HEMT is an excellent substitute to the currently used MIS-HEMTs for delivering high power density and frequency at RF/power amplifier applications.

Keywords: *Enhancement mode, Hydrodynamic simulation, InN channel, MIS-HEMT, $In_{0.9}Al_{0.1}N$ barrier/buffer, HfO_2, T_{CH}, Transconductance*

1. INTRODUCTION

For nearly 50 years, the microelectronics revolution has been characterized by "smaller is better," the amazing realization that scaling down transistor size leads to increased transistor density, faster switching speed and enhanced power efficiency. A significant turn in this exhilarating ride took place in the last few years. Si CMOS scaling is now in a new phase of "power constrained scaling" in which the power density dissipated by logic CMOS chips has all but hit a limit of about 100 W/cm2 [1]. Power density cannot increase much more without incurring in very substantial packaging and cooling costs that are impractical for most applications. Under power constrained scaling, continued transistor size scaling demands a reduction in operating voltage [2]. Trying to accomplish this while enhancing transistor performance has become increasingly difficult. Partly because of this, the operating voltage for CMOS has bottomed at around 1 V for the last few generations of technology. This hard limit poses a serious threat to further progress.

One way out of this is by introducing a new channel material with a much higher carrier velocity. This would allow further voltage scaling while continuing to enhance performance. A promising family of materials is III-V compound semiconductors. III-Vs are well known for their unique suitability for high frequency electronics. III-V based integrated circuits are now widely used in communications and defense applications. Some of these are mission critical, such as space systems where exceedingly high reliability is essential. Others are mass-market and very cost-sensitive applications such as low-noise amplifiers and switches for smart phones. Of all alternatives that are being considered to extend the life of CMOS, III-Vs are

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the only materials with an established manufacturing and reliability record.

High electron mobility transistors (HEMT) based on the III-V semiconductors GaAs and InN are very popular and successful devices for radio frequency and power applications [8]. The operating frequencies of these transistors cover the range from 800 MHz to **1** THz. About 3O years ago, a new HEMT type based on the wide bandgap material GaN has been introduced – the GaN High Electron Mobility Transistors (HEMTs). Since that time, GaN HEMTs have attracted a lot of attention. GaN technology has been steadily improved and each year GaN HEMTs with new RF record performance have been reported. Today, these devices show output power densities superior to any other RF field-effect transistor (FET) type, and are very promising candidates for high-power amplification in the frequency range up to 1 THz (and possibly above). The frequency limits (cut-off frequency and maximum frequency of oscillation,) of GaN HEMTs have been pushed beyond 1 THz recently [l1]. The impressing power and frequency performance of GaN HEMTs is due to some unique material properties of the AlGaN/GaN material system.

InN is a unique material with the highest electron velocity among all common semiconductors, about four-times higher than for Si [1, 2]. Consequently, high mobility binary InN-channel transistors may substantially outperform speed performance of Si-based devices. Besides that, InN belongs to a family of III–V semiconductors which are polar materials with an ability to create high-density Two-Dimensional Electron Gas ($_{2DEG}$) in a quantum well (QW) of high-electron mobility transistors (HEMTs) without intentional doping [3]. InN-based HEMTs may be record fast among III-V transistors. [4,5]. Theoretical analysis has shown that, for ideal transistors with L_g = 0.1 μm, by replacing the GaN channel with InN, we can expect f_T to increase from 480 to 880 GHz [6].

There are several advantages associated with GaN based devices, such as lower contact resistance [8], better channel confinement [9], and enhancement mode operation [10]. In conjunction with a strain-free lattice matched InAlN back-barrier confinement layers with record high transconductance and power gain cutoff frequency has been reported [11,12]. Thus, GaN technology has evolved as a viable candidate for an ultra-scaled GaN HEMT technology. Great progress has been made towards good DC and RF performance in GaN-based HEMTs. Finally, the SiN_x/AlGaN/GaN/AlGaN MISHEMT with f_t/f_{max} of 103/196 for V_{ds} = 5.5 V along with high ON-state resistance of 1.02 Ω·mm was reported for GaN device grown by metal-organic chemical vapor deposition [17]. Unfortunately, there are few devices developed for E-mode HEMT's with positive threshold (V_T) and high transconductance (g_m) [13,16]. The device with V_T can secure safe operation of the device while transconductance may provide excellent high-frequency performance [18]. The device aspect ratio L_g/T_{CH} plays key role in predicting the short-channel effect [19]. It has a direct effect on the DC and RF characteristics. To suppress the short channel effect, a critical aspect ratio has to be held to suppress the short channel effect. To maintain proper electrostatics and retain a relatively high aspect ratio, the gate dielectric and channel thickness need to be scaled along with the gate length [19] to improve high RF performance in nanometer scale gate length. In this paper, we report the device performance of a E-mode HfO_2 -GaN/InN/GaN/$In_{0.9}Al_{0.1}N$ heterostructure MIS-HEMTs with scaled gate dielectric and InN channel thickness. This work present devices with great potential for RF/power amplifier amplifications by achieving high V_T, g_m and high frequency performance (f_t / f_{max}) simultaneously.

Thus, the objective of this study is to investigate the impact of InN channel thickness (t_{InN}) and HfO2 as dielectrics on the normally-OFF GaN/InN/GaN/$In_{0.9}Al_{0.1}N$ heterostructure MIS-HEMTs so as to achieve high $I_{ds,sat}$, V_T, g_m, f_t and f_{max} and low intrinsic delay (τ), ON-state resistance (R_{ON}) under low voltage bias due to effect of polarization-induced charges at all of the interfaces. Because of the immature state of the InN heterostructures, this type of devices exists only as a theoretical concept [18, 20] and till now no optimization and performance along with the electrical properties of the device were carried out

2. DEVICE ARCHITECTURE

Fig 1 shows the GaN/InN/GaN/$In_{0.9}Al_{0.1}N$ heterostructure MIS-HEMT used in this research. The bottom layer is an 0.6 μm GaN layer, followed by a relaxed 1 μm $In_{0.9}Al_{0.1}N$ back-barrier/ buffer layer. On top of this, a strained 0.6 nm GaN spacer is placed. The role of this spacer is to confine the channel electrons and to screen possible alloy disorder scattering effects coming from the $In_{0.9}Al_{0.1}N$ buffer [21]. The lattice matched composition of $In_{0.9}Al_{0.1}N$ layer makes an excellent choice for the buffer to improve channel conductivity in devices [12]. The

active InN channel with T_{CH} varies from 0.3 – 2 nm, which is strained with an additional strained 0.4 nm GaN spacer on top. This second GaN spacer provides a negative polarization charge at the upper interface of the channel which depletes it from electrons when no gate voltage is applied. Hence, the second spacer that makes the device a normally-OFF transistor. A gate insulator, HfO_2 ($\kappa \sim 21$) with t_{ins} = 4 nm is used below the gate. In addition to the structure, doped regions with $N_D = 1\times10^{20}$ cm^{-3} were added around the source and drain in order to assure a good contact with the InN channel. The device has a gate length L_g = 100 nm, source-gate extension and a gate-drain extension L_{sg} = 0.5 µm and L_{gd} = *1* µm. The values of the interface polarization charges in the normally-OFF structure are listed in Table 1. Traps were included in the back-barrier and buffer layers to make the substrate semi-insulating.

Table 1: Polarization charge density at each interface [18]

Parameter	Interface polarization charge N_{it}
HfO_2/GaN interface	~ 10.1× 10^{13} cm^{-2}
Upper GaN/InN interface	~ -9.5× 10^{13} cm^{-2}
InN/ lower GaN interface	~ 9.5× 10^{13} cm^{-2}
GaN/$In_{0.9}Al_{0.1}N$ interface	~ -7.8× 10^{13} cm^{-2}

3. SIMULATION PROCEDURE

The simulation of the device was performed using the Sentaurus TCAD K-2015 simulator [22]. The hydrodynamic (*HD*) transport model that accurately considers the non-equilibrium conditions such as quasi-ballistic transport in the thin regions and velocity-overshoot affect in the depleted regions and the dependence of impact ionization rates on carrier energy distributions was used for device simulation. Several important physical effects such as bandgap narrowing, variable effective mass and doping dependent mobility at the high electric field was also accounted in the simulations [23]. Arora doping dependence mobility model [23] was used to model the effect of mobility, electric field and the carrier temperature. Shockley carrier recombination model, stain and stress polarization model [24, 25] are considered to determine the carrier lifetime and the density in a precise way.

4. RESULTS AND DISCUSSIONS

For accurate device simulation, the physical model parameters for transport model are well-matched to the reported measured data [13, 18] as shown in Fig. 2 and Fig. 3. In addition, an optimized device meshing was used to generate robust simulation structures prior to the calibration of physical models. The detailed device meshing and calibration procedure is described elsewhere [26]. The calibrated physical models are used to simulate the device described in Fig.1 and obtain different device characteristics as described below.

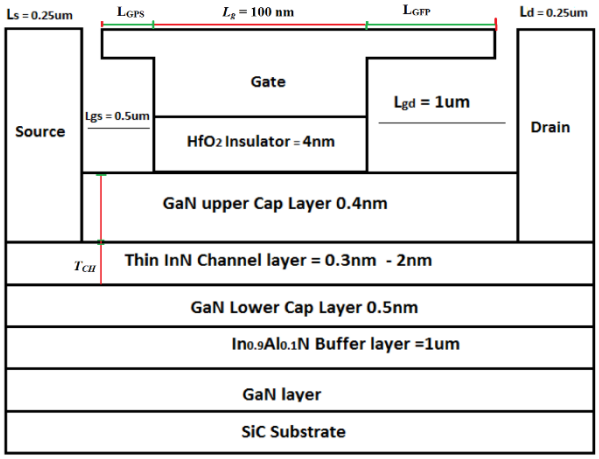

Fig.1 Cross-section of highly confined HfO_2/GaN/InN/GaN/$In_{0.9}Al_{0.1}N$ MISHEMT structure used for numerical device simulation. L_g, L_{gs} and L_{gd} are the gate length, S/D access region lengths, respectively. T_{CH}, a is the channel thickness and gate to channel distance.

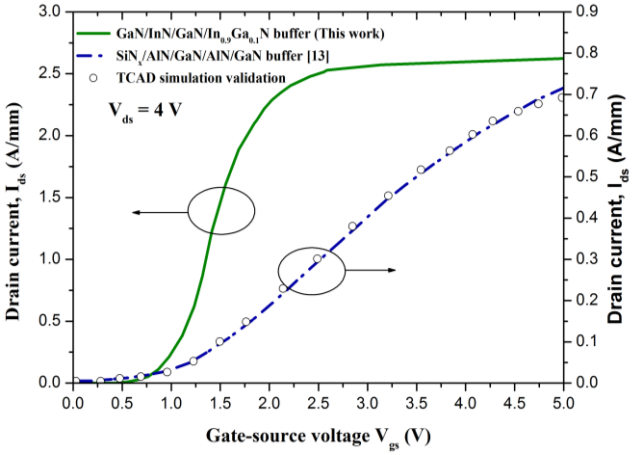

Fig. 2. Experimental [13] (solid dotted lines) and simulated (symbols) transfer characteristics for AlN/GaN/AlN MISHEMT after tuning the simulation model to match the experimental curve with our InN channel MISHEMT.

Fig. 4 shows the simulated conduction energy band diagram of the various regions of the device and electron concentration profiles in the channel under the gate for GaN/InN/GaN/$In_{0.9}Al_{0.1}N$ heterostructure MIS-HEMT for InN channel thickness (T_{CH} = 3 nm). Under the gate, the band-diagram shows that the 2-DEG is completely depleted by the top GaN layer and the device will be normally-OFF. For the normally-OFF structure, a negative interface trap density N_{it} ~ - 5 $\times 10^{13}$ cm^{-2} was included at the HfO_2/GaN interface [18] which lowers the positive polarization charge.

Fig. 5 shows the DC I_{ds} versus V_{ds} characteristics of the HfO_2/GaN/InN/GaN/$In_{0.9}Al_{0.1}N$ devices described in section II. The saturated drain current ($I_{ds,sat}$) of 2.7, 2.38, 2.09, 1.39, 0.78, 0.315 A/mm is obtained at V_{gs} = 1.6 V and V_{ds} = 5 V for devices with T_{CH} = 3, 2.5, 2, 1.5, 1 and 0.5 nm, respectively. This high value of $I_{ds,sat}$ is attributed to the superior electron mobility and conductivity in the InN channel.

Fig. 6 shows the I_{ds}-V_{gs} characteristics of a L_g = 100 nm InN channel MISHEMT for V_{gs} from -1 V to 2 V and V_{ds}= 0.5 V with T_{CH} as the third parameter. The simulation data show that for T_{CH} = 0.5, 1, 1.5, 2, 2.5 and 3 nm the values of $I_{ds,sat}$ are 1.17, 2.08, 2.18, 2.47, 2.52 and 2.57 A/mm, respectively. It indicates that the current through the channel will become a significant or larger component of the total drive current as the V_{gs} increases. The increased current capability is due to the presence of high mobility InN channel with high *2DEG* induced close to their interfaces, respectively under a 0.5 V gate bias. From Fig. 8, it has been seen that the V_T begins to shift positively as the T_{CH} decreases and device leakage current can be significantly reduced by using high-*k* dielectrics or thin T_{CH}. The proportion of the amount of the charges in the channel region controlled by the V_{gs} is increased. V_T increases almost linearly from 0.102 V for T_{CH} = 3 nm to 0.728 V for T_{CH} = 0.5 nm.

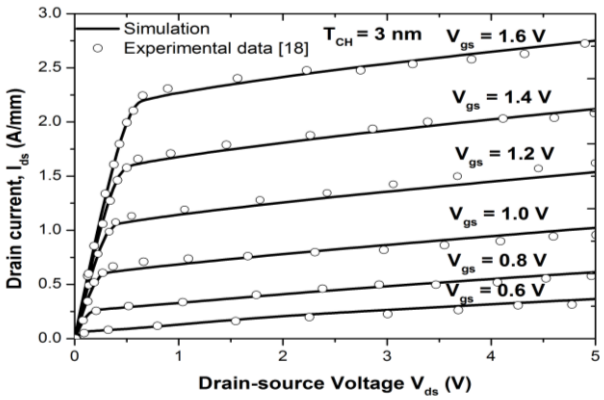

Fig. 3. Experimental [18] and simulated I_{ds}-V_{ds} curves for InN channel MISHEMT with T_{CH} = 3 nm. The gate voltage was varied from 1.6 V to 0.6 V in step of 0.2 V.

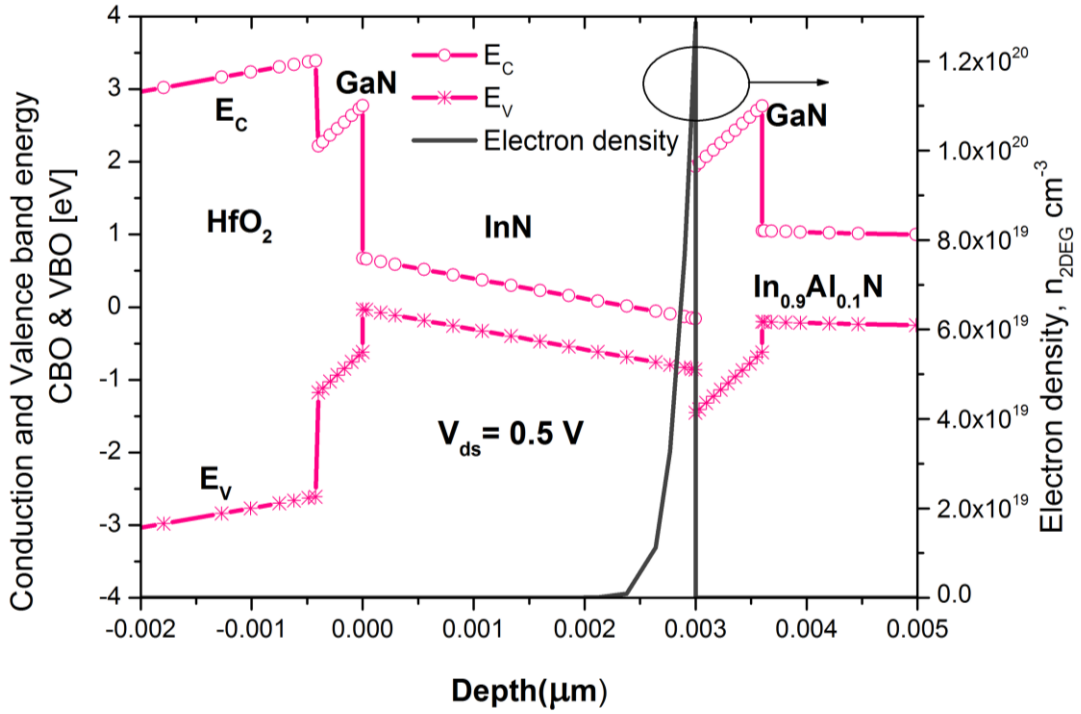

Fig. 4. Simulated conduction energy band diagram and electron density of the device under the gate. The thickness of InN channel is T_{CH} = 3 nm. There is relaxed 1μm $In_{0.9}Al_{0.1}N$ buffer layer with GaN top and bottom cap layers.

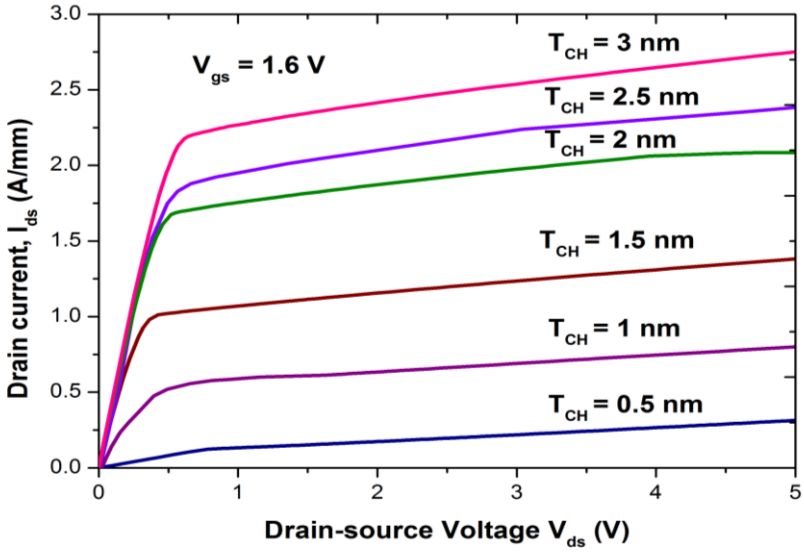

Fig. 5. I_{ds} as a function of V_{ds} in InN MISHEMT with various T_{CH} measured at V_{gs} = 1.6 V.

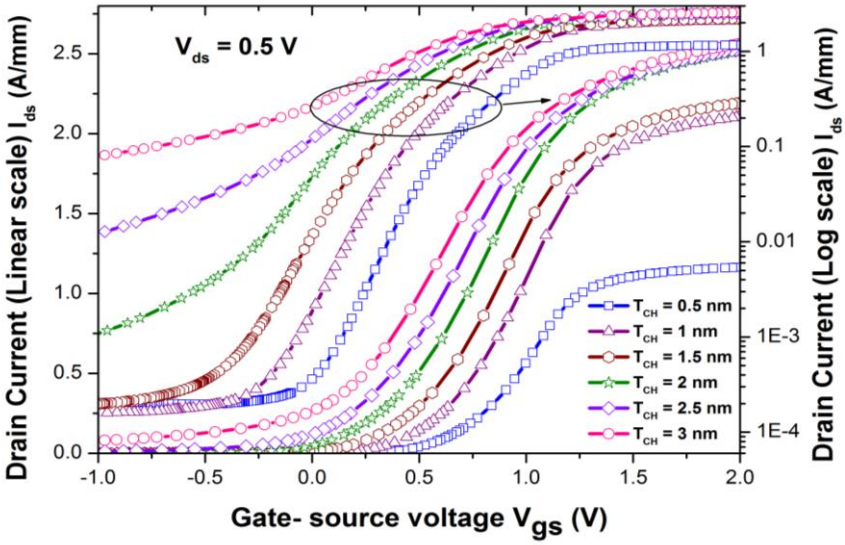

Fig. 6. Simulated transfer characteristics of I_{ds} versus V_{gs} (both linear and log scale) for various values of T_{CH} in the InN channel measured at V_{ds} = 0.5 V.

Fig. 7 shows the variation of g_m as a function of V_{gs} at V_{ds} = 0.5 V. From Fig. 7, it is found that the values of maximum g_m for InN channel MISHEMT with L_g =100 nm is 2.9, 2.81, 2.76, 2.71, 2.58 and 2.44 S/mm for the values of T_{CH} = 0.5, 1, 1.5, 2, 2.5 and 3 nm, respectively. The device with thicker channel (T_{CH}) presents a wider current path and higher 2-DEG density, resulting in a more negative V_T as well as a decreased peak transconductance [27].

An I_{ON}/I_{OFF} ratio is a commonly evaluated merit for current technology. This ratio has a significant impact on the static power consumption in low standby power applications and higher values of the I_{ON}/I_{OFF} ratio are desirable.

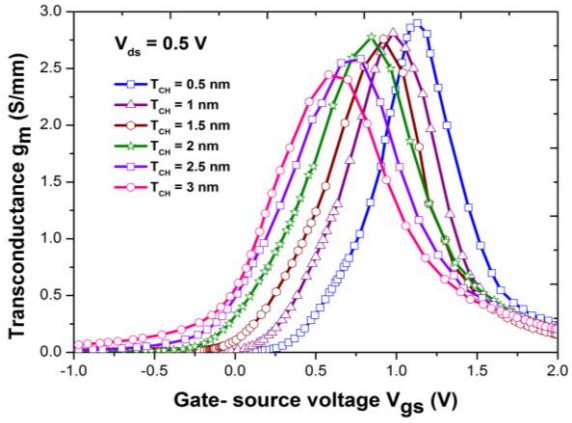

Fig. 7. Variation of g_m as a function of V_{gs} characteristics for various values of T_{CH} in InN channel varying from 0.5 nm to 3 nm at V_{ds} = 0.5 V.

The *ON*-current refers to the drive current in saturation, while *OFF*-current refers to the total leakage current, which is the sum of subthreshold, gate and junction leakage currents [28] extracted from I_{ds}–V_{gs} transfer characteristics at V_{ds} = 0.5 V and V_{gs} = 0 V for I_{OFF}, V_{gs} = 2 V for I_{ON} shown in Fig. 8. It clearly shows that *ON* current and OFF current is higher for device with higher T_{CH} due to increased 2DEG along with high gate to channel separation [29]. The threshold voltage dependence on T_{CH} is shown in Fig. 8. As seen in Fig. 8, the V_T decreases with increasing T_{CH} for a given gate length device. As T_{CH} increases, V_T decreases and becomes more negative due to the increased gate-to-channel distance shown in Fig 8 and achieved a maximum positive V_T = 0.828 V, 0.635 V, 0.494 V, 0.360 V, 0.208 V, 0.102 V for the values of T_{CH} = 0.5, 1, 1.5, 2, 2.5 and 3 nm, respectively. We have also seen that V_T shifts positive as the T_{CH} is thinned down. The positive V_T is desired for low-power and enhancement-mode operation.

Fig. 9 shows the ON-state resistance (R_{ON}) of device with respect to T_{CH}. For this, the simulation was first performed to obtain the I_{ds}-V_{ds} characteristic in the DC mode for the values of T_{CH} = 0.5, 1, 1.5, 2, nm with a step of 0.5 nm. The device R_{ON} extracted at V_{gs} = 1.6 V and V_{ds} in the range between 0 and 0.21 V from Fig. 4. The R_{ON} of the device should be very low to reduce the power consumption in the device switching process. R_{ON} was found to decrease linearly as n_s increases [30] and is given by

$$R_{ON} = \frac{L_{gd}}{qn_s\mu} \quad (1)$$

where L_{gd}, q, n_s and μ are the gate to drain access region length, the electron charge, electron sheet carrier density and mobility of the device, respectively. This causes a high device R_{ON} with decreasing 'T_{CH}' in the device. We see an increase in R_{ON} from a value of 0.242, 0.25, 0.277, and 0.41 Ω·mm for 2, 1.5, 1, 0.5 nm, respectively. Due to the low channel resistance of the InN channel MISHEMT, the values are low compared to what has been published so far [13,16,17].

Fig. 10 shows the variation of high frequency (1 MHz) *C-V* characteristics of the device for various values of T_{CH} with respect to V_{gs}. For MISHEMT devices the total gate capacitance (C_{gg}) can be given as

$$C_{gg} = Series(C_{ins} + C_{cap}) \,||\, C_{gs} \,||\, C_{gd} \quad (2)$$

where $C_{ins} = \varepsilon_0 \times \varepsilon_{ins} \times A/t_{ins}$

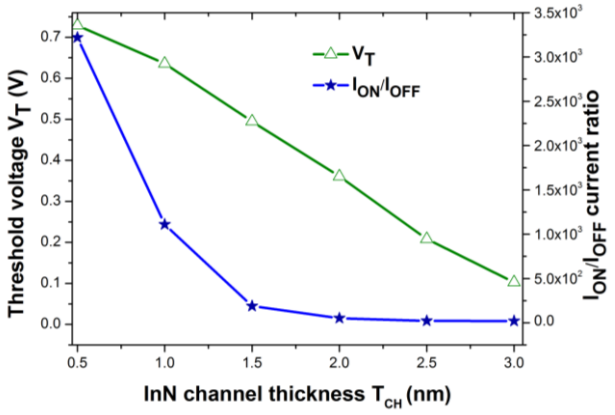

Fig. 8. Variation of V_T and I_{ON}/I_{OFF} as a function of various T_{CH} in InN channel measured at V_{ds} = 0.5 V.

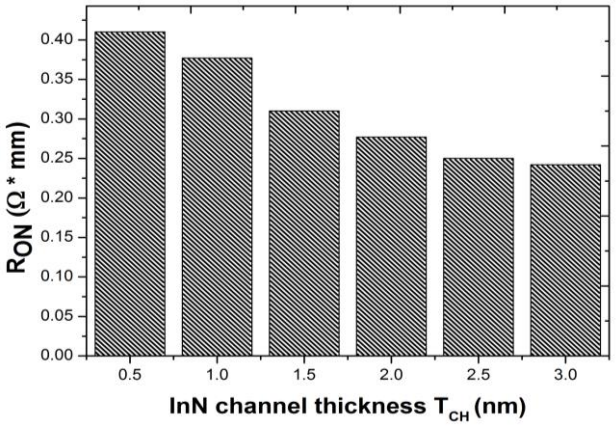

Fig. 9. Variation of ON-state resistance R_{ON} as a function of T_{CH} varying from 0.3 – 2 nm measured from I_{ds}-V_{ds} characteristics at V_{gs} = 1.6 V.

C_{ins} is the insulator capacitance, C_{cap} is the depletion layer capacitance comprises of GaN cap top and bottom layers with InN channel, ε_O is the vacuum permittivity, ε_{ins} is the dielectric constant of high-*K* HfO_2 dielectric, and *A* is the capacitor area. C_{gs} and C_{gd} are the gate to source and gate to drain capacitances respectively. C_{gs} and C_{gd} include the inner (C_{if}) and outer (C_{of}) fringing capacitances. It is noticed that there is almost negligible effect of T_{CH} on C_{gg} before threshold and at strong inversion the capacitance is slightly higher for higher T_{CH}. This is because in wider channel the carrier confinement is better which gives rise to higher C_{gg} [31].

The intrinsic delay time (τ) of a transistor is the time taken to charge a constant gate capacitance C_{gg} to a voltage V_{ds} at a constant drain current I_{ON} [32]. The τ is a most important figure of merit because it determines the device switching speed depends on mobility and injection velocities of carriers, which are high in case of III-V materials [2] and is given as,

$$\tau = \frac{C_{gg} \times V_{dd}}{I_{ON}} \quad (3)$$

where C_{gg} the total gate capacitance, $V_{dd} = V_{ds}$ is the supply voltage and I_{ON} is the ON current for various T_{CH}. Due to higher I_{ON} in MIS-HEMT devices, the τ will be very less and fast device switching can be achieved. Thus, MISHEMTs will have much lower C_{gg}, leading to the further reduction of delay. Lower values of the τ are highly desirable for logic systems and applications requiring high-performance operation [32]. Delay decreases almost linearly from 1.661 Fs for T_{CH} = 0.5 nm to 0.761 Fs for T_{CH} = 3 nm shown in Fig. 11.

Another important figure of merit for RF application is that cutoff frequency f_t and the maximum frequency of oscillation f_{max} which depend on the C_{gg} and g_m of a device The f_t is the frequency when the current gain is unity and is an important measure for high speed digital applications, whereas f_{max} is the frequency when the power gain is unity and also corresponds with the transit frequency of the maximum available power gain (*MAG*) that is a realistic parameter of the optimization of microwave amplifiers. The f_t and f_{max} can be given as [33]

$$F_t = \frac{g_m}{2\pi C_{gs}\sqrt{1+2(C_{gd}/C_{gs})}} \approx \frac{g_m}{2\pi(C_{gd}/C_{gs})} \approx \frac{g_m}{2\pi C_{gg}} \quad \text{- (4)}$$

$$F_{\max} = \frac{g_m}{2\pi C_{gs}\sqrt{4(R_s+R_i+R_g)(g_{ds}+g_m(C_{gd}/C_{gs}))}}$$

where C_{gs}, C_{gd} and $C_{gg} = C_{gs} + C_{gd}$ are the gate-to-source, gate-to-drain and total gate capacitances respectively, including fringing and overlap capacitances, g_m and g_{ds} are the transconductance and output conductance, R_g, R_S and R_i are the gate, source and channel resistance.

Fig. 11 show the variation of f_T and f_{max} for different values of T_{CH} of an L_g = 100 nm device. Fig. 11 clearly exhibit an increase in f_T and f_{max} with the reduction of T_{CH}. This increase in f_T and f_{max} is due to the increase in g_m as T_{CH} is scaled down. The highest values of f_T / f_{max} observed are 98 GHz/129 GHz and 200GHz/360 GHz for L_g = 100 nm devices with T_B = 0.5 nm at V_{ds} = 0.5 V and 1.0 V, respectively. The higher f_t and f_{max} for the thin channel device (T_{CH} = 0.5 nm) is due to the superior gate-controllability, and hence higher g_m and lowest parasitic gate capacitances compared to the thick channel (T_{CH} = 1, 1.5, 2, 2.5, 3 nm) that results from increased gate capacitance [34].

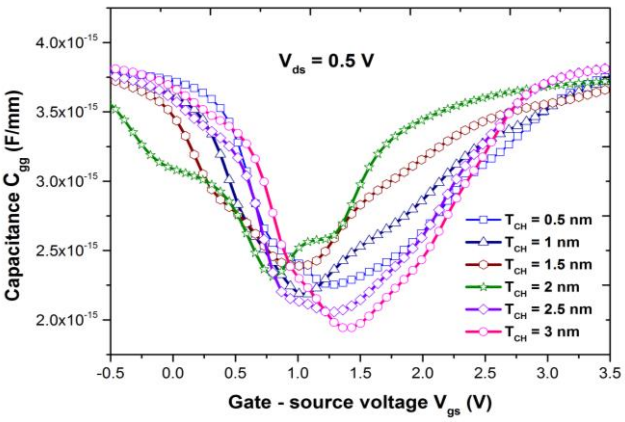

Fig. 10. Gate capacitance C_{gg} of the 100 nm gate InN channel MISHEMT as a function of various T_{CH} with V_{ds} = 0.5 V.

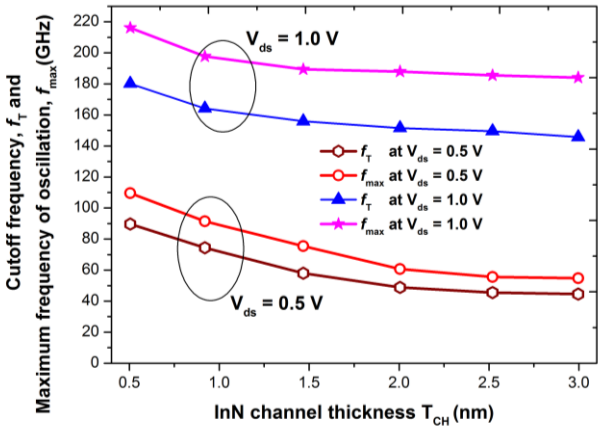

Fig. 11. Variation of f_t and f_{max} for various T_{CH} with L_g = 100 nm at V_{ds} = 0.5 V and V_{ds} = 1.0 V.

5. CONCLUSION

The effect of the thickness of InN channel T_{CH} were studied and analyzed and the successful improvement of device performance of the normally-OFF operation was achieved due to the introduction of HfO_2 as gate dielectrics of the GaN/InN/GaN/$In_{0.9}Al_{0.1}N$ heterostructure. Significant increase in *2DEG*, I_{ON}, g_m, demonstrates the presence of high current density in the device channel material due to the presence of HfO_2 dielectrics which significantly reduces the current leakage under gate of the device. In addition, incorporation of the strain-free lattice matched $In_{0.9}Al_{0.1}N$ back-barrier design in E-mode technology provides more flexibility and improvement of E-mode operation of the device. As T_{CH} becomes thinner, the RF performance of the devices improved and an impressive f_T/ f_{max} peak values of 98 GHz/129 GHz and 200 GHz/360 GHz, respectively, for L_g = 100 nm at V_{ds} = 0.5 V and 1 V was achieved as against the conventional heterostructure. Furthermore, high frequency performance is possible under high voltage

biases and it can be a promising device structure for RF/power amplifier applications.

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