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HYBRID MODULATION SCHEME FOR CASCADED H-BRIDGE INVERTER CELLS

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ABSTRACT
This work proposes a switching technique for cascaded H-Bridge (CHB) cells. Single carrier Sinusoidal PWM (SCSPWM) scheme is employed in the generation of the gating signals. A sequential switching and base PWM circulation schemes are presented for this fundamental cascaded multilevel inverter topology. With these proposed concepts, it is now possible to generate equal average switching signal patterns in all the constituting power semiconductor switches. This results in equal switching loss dissipation and equal power sharing in CHB multilevel inverter modules; and therefore technically modularizes the cascaded system. A 4-cell cascaded structure has been used to exemplify the proposed switching technique. Outlines with switching functions are given for the proposed modulation strategy. For a modulation index of 0.9, a THD value of 14.62% has been achieved in the output voltage waveform of the exemplanary 4-cell cascaded configuration. Verification of the performance of the proposed control technique is done through simulations and experiments.

Keywords: *Cascade H-Bridge, multilevel, PWM, H-bridge.*

1. INTRODUCTION
One of the most significant recent advances in power electronics is the multilevel inverter. Using this concept, the power conversion is performed with enhanced power quality. In this scenario, the diode-clamped, flying-capacitor, and cascaded H-bridge multilevel inverters were proposed to replace the traditional three-level inverters in medium and high-voltage level applications such as motor drives and static var compensators [1]–[10]. Akagi, [11], shows one way of classifying multilevel inverters, similar to the classification by Lai and Peng [12].

Three different basic multilevel inverter topologies are the neutral point clamped (NPC) or diode clamped [1], the flying capacitor (FC) or capacitor clamped [3] and the cascaded H-bridge (CHB) [5]. The main drawbacks of NPC inverter topology, with a level number higher than 3, is the necessity of a capacitor voltage balancing control circuit and the high voltage across the clamped diodes. The FC multilevel inverter uses flying capacitors as clamping devices. These topologies have several attractive properties in comparison with NPC inverters, including the advantages of the transformerless operation and redundant phase leg states that allow the switching stresses to be equally distributed between semiconductor switches [13]. But these inverters require excessive number of storage capacitors for high voltage steps. A double FC multi-cell inverter has been presented in [14]. This topology has been implemented by adding two low-frequency switches to the conventional configuration of the FC multilevel inverter. The main advantages of the presented inverter in comparison with the FC multilevel inverter are the doubling of the rms value of the output voltage and the number of voltage steps and the cancelling of the midpoint of the dc source. But two additional switches must operate at the peak of the output voltage. This restricts high voltage applications of this inverter. The series connection of several basic H-bridge inverters results in the multilevel cascaded H-bridge (CHB) inverter configurations, which have attractive attributes, [15] - [18]. This inverter topology is proper option for high level applications from the point of view of modularity and simplicity of control.

In recent years, several topologies with various control techniques have been presented for cascaded

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multilevel inverters [19]-[23]. Moreover, asymmetric and/or hybrid multilevel inverters have been presented in [24], [25]. In asymmetric topologies, the values of the dc voltage source magnitudes are unequal or change dynamically [26]. These converters reduce the size and cost of the converter and improve the reliability, since fewer semiconductors and capacitors are employed [27]. The hybrid multilevel converters are composed of different multilevel topologies with unequal values of dc voltage sources and different modulation techniques and/or semiconductor technologies. With appropriate selection of switching devices, the converter cost is significantly reduced. But, the application of different multilevel topologies results in total loss of modularity and produces problems with switching frequency and restrictions on the modulation and control method [28].

One of the salient factors that determine the performance of cascaded multilevel inverters is their control techniques. These control strategies are based on the following conventional methods: sinusoidal PWM (SPWM) extended to single and multiple carrier arrangements, space-vector PWM (SVPWM), non-sinusoidal carrier PWM, selective harmonic elimination PWM (SHEPWM), [29]-[44]. Application of these control techniques results in cascaded multilevel inverters synthesizing output voltages with very low Total Harmonic Distortion, THD. But they do not take into account that cascaded inverter cells should equally share the overall output power.

A typical case is seen in the conventional control of the CHB multilevel inverter topology whose 9-level power circuit is shown in figure 1. The output voltage and power profiles are shown in figures 2 and 3. Figure 3 clearly shows that different powers are drawn from different dc voltage sources. And also indicate that the cells are not actually modularized. As a result, there is then the need for the allocation of different rated power circuit components and dc sources to respective cascaded cells during the design process; thus, negating the proposed concept of cascading similar inverter cells with the same characteristics and power capabilities. Works done in [45] and [46] proposed switching strategies to balance the switching loss dissipation among the four switches in a given cell but not in all the constituting power switches of the cascaded system.

Based on these technical backgrounds, this paper presents a control strategy, based on the single-carrier multilevel modulation technique, [47], which ensures equal power handling capability in CHB multilevel inverter modules. Besides, a sequential switching scheme is embedded in this proposed control method to overcome differential heating among the cascaded cells due to unequal power loss dissipation. In this control technique for the cascade structure, the voltage pulses made in different CHB inverter unit cells in a period rotate between these cells in a way that after n periods, all the cascaded modules receive the same average switching signals; where n is the number of cascaded unit cells.

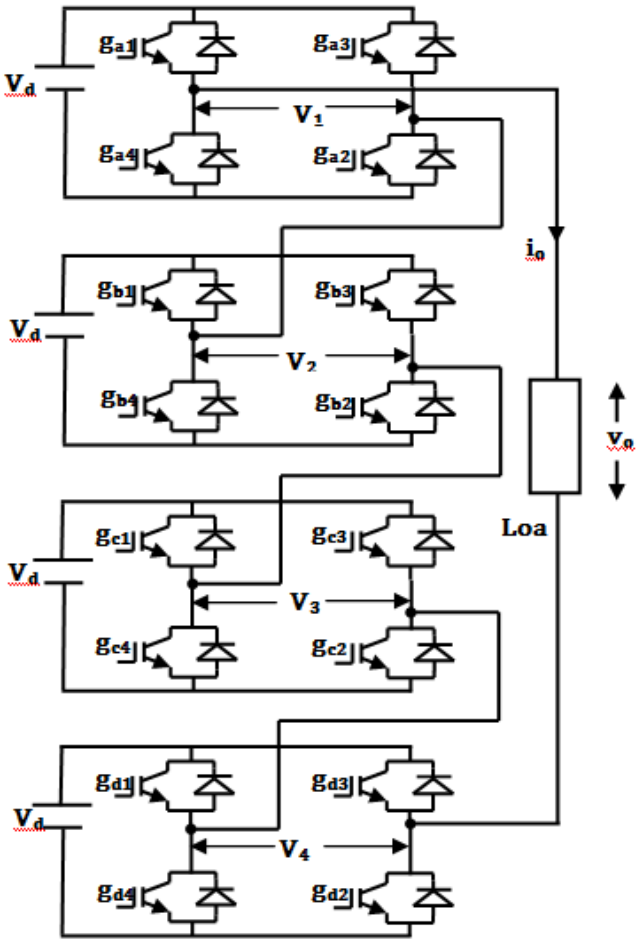


Figure 1: Configuration of 9-level cascade H-bridge multilevel inverter.

In this article, four CHB inverter unit cells have been used to verify the performance of the proposed switching scheme. However, the proposed modulation strategy can equally be extended to any number of cascaded cells. Operational principles and switching functions are analyzed. Simulation and experimental results are presented to verify the validity of the proposed switching technique.

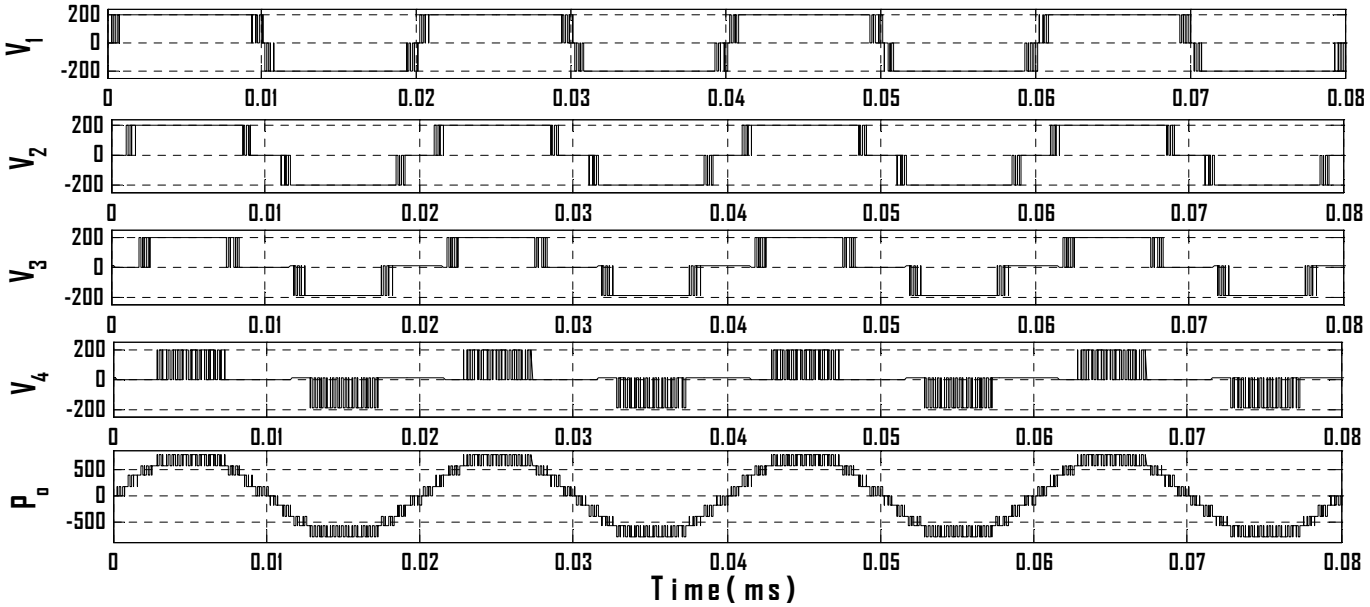


Figure 2: Voltage profile f the 9-level CHB inverter with the conventional design

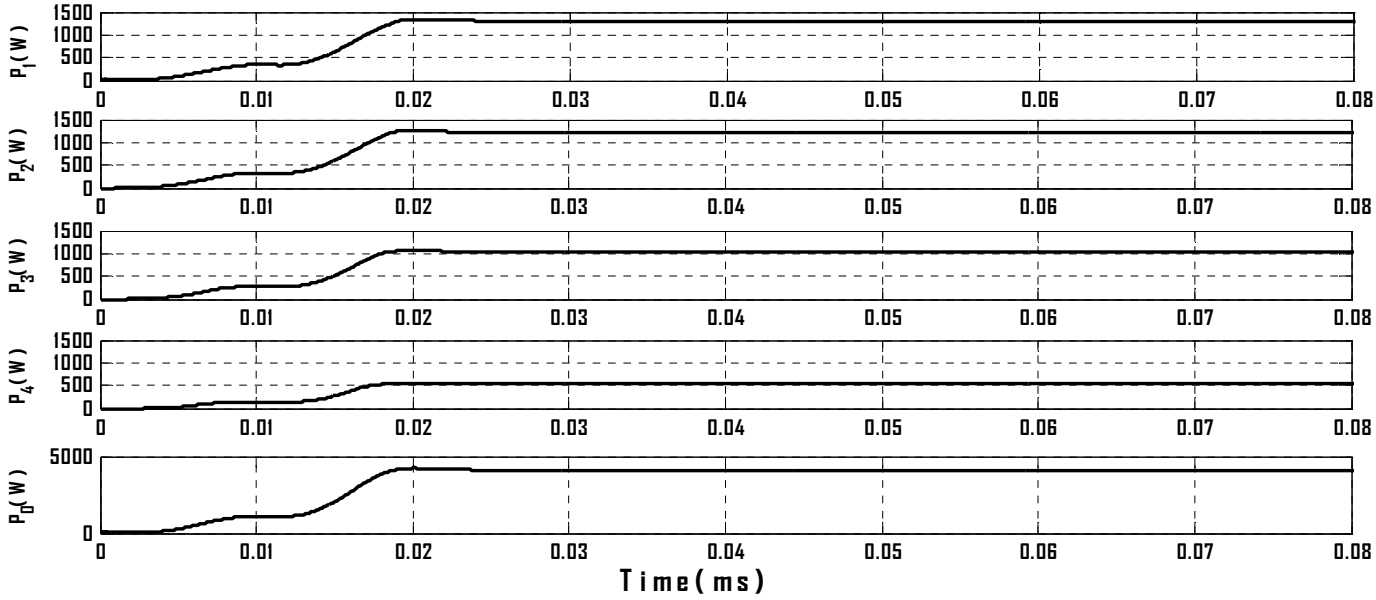


Figure 3: Power profile of the 9-level CHB inverter under the conventional control method

3. PROPOSED PWM SWITCHING SCHEME

Single carrier Sinusoidal PWM (SCSPWM) scheme is employed in the generation of the gating signals. Basic principle of the proposed switching strategy is to generate gating signals by comparing rectified sinusoidal modulating/reference signals, at the fundamental frequency, with only one triangular carrier wave at the desired switching frequency. *2n* rectified sinusoidal modulating signals have the same fundamental frequency, f_m, and amplitude, A_m, with dc bias of A_c (peak-peak amplitude of the triangular carrier signal) as a difference between these signals, for *k*-level SCSPWM. If *k* is the number of voltage level synthesized, per half-cycle, the frequency and amplitude modulation indices expressions, [40], [48], are given as:

$$M_f = \frac{f_c}{f_m} \tag{1}$$

$$M_a = \frac{A_m}{A_c(k-1)} \tag{2}$$

Figure 4 shows the general structure of the proposed switching scheme for the cascaded multilevel inverter shown in Figure 1. It consists of the base switching signal, module signal equalizing generator and gating signal sequence generators.

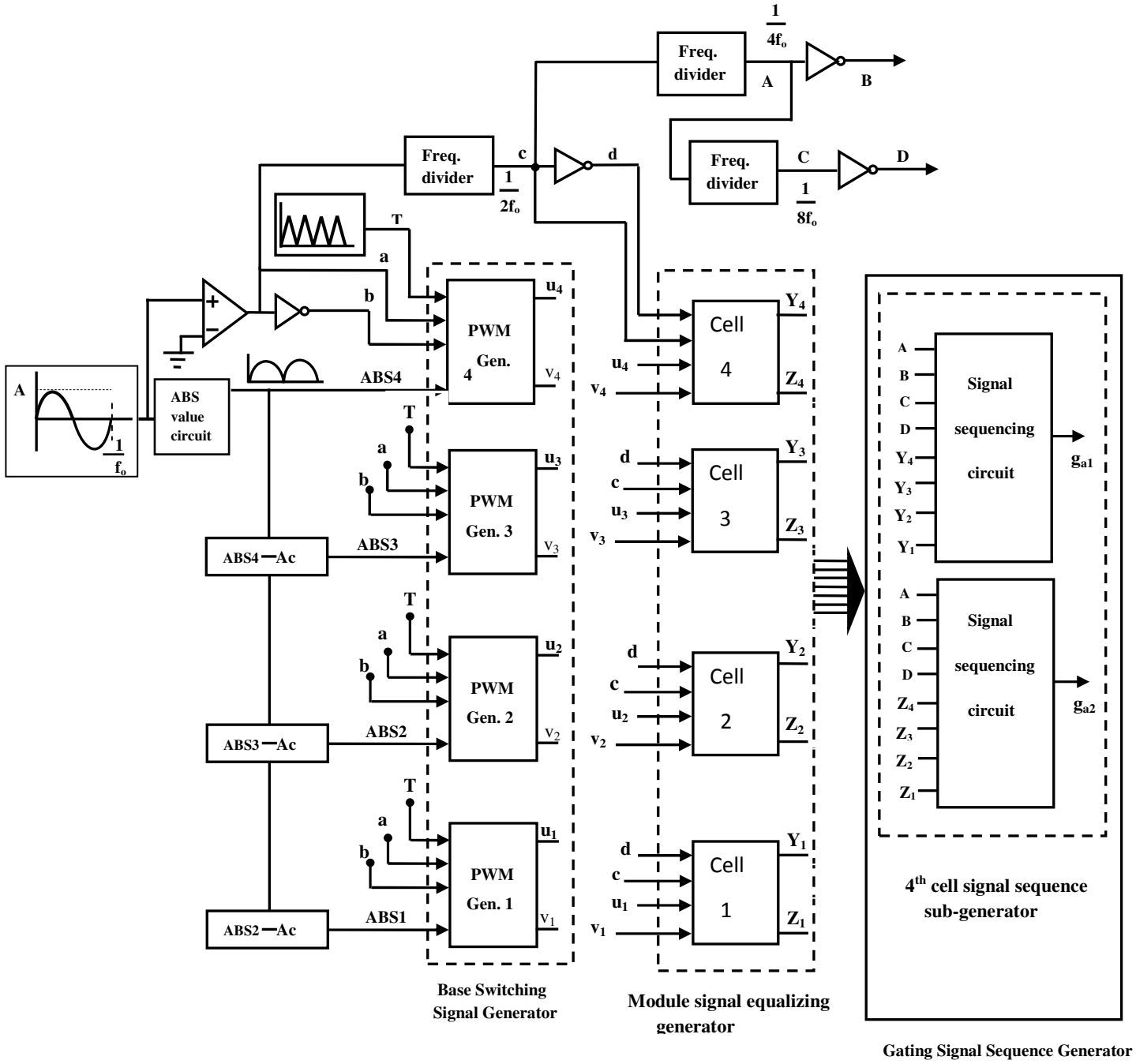


Figure. 4: Switching patterns of the proposed modulation strategy.

3.1 Base Switching Signal Generator

The Base Switching Signal Generator comprises of *n* modulators; each synthesizing the respective base firing pulses. Each base signal generator receives a common single-carrier triangular wave, T, a rectified reference signal, two common square wave signals at fundamental frequency and with 50% pulse width, a and b. PWM signals, u_i , v_i , i=1,2,3,4, are obtained by the comparison of the reference waveform of each module with the carrier waveform. Considering the uppermost H-bridge inverter unit cell in figure 1, the logic expressions for the base signal u_4 *and* v_4 are:

$$u_4 = \left[\left(ABS4 > T \right) . \, a \right] \tag{3}$$

$$v_4 = \left[\left(T > ABS4 \right) . \, b \right] \tag{4}$$

where ABS is the mathematical/logical absolute value. Similar logic expressions can be derived for the base signals of the other cascaded modules.

3.2 Module Signal Equalizing Generator

Precisely, this generator ensures that in a particular H-bridge module, all the four power switches receive averagely equal gating pulses. In other words, equalization of switching/conduction losses among the power switches of a given H-bridge module is accomplished within this generator. Each sub-generator is fed with the two corresponding PWM signals from the base switching signal generator and two common square wave signals at half the fundamental frequency and with 50% pulse width, c and d. Taking the uppermost H-bridge inverter unit cell in figure 1, the logic expressions for this generator corresponding to this module are:

$$Y_4 = \left[\left(u_4 + v_4 \right) \bullet c + a \bullet d \right] \quad (5)$$

$$Z_4 = \left[\left(u_4 + v_4 \right) \bullet d + a \bullet c \right] \quad (6)$$

3.3. Gating Signal Sequence Generator

For long operating-time expectancy and also to modularize the inverter system, it is important to equally share the overall output power among the cascaded modules. This is the key issue the proposed modulation scheme in figure 3 covers. The sequence generator ensures that all similar generated switching signals in section 3.1, in the *n* cascaded modules, are made to appear in each of the gating pulses of all similar power switches in the cascaded structure in a well defined sequence. This generator is made up of *n* sub-generators and each of these sub-generators comprises of three Signal Sequencing Circuits. Each of the signal sequencing circuit is an array of logic AND and OR operations. Referring to figure 4, the inputs to this generator are: all the generated waveforms from the module signal equalizing generator in section 3.2, four square wave signals with 50% pulse width and at frequencies of $\frac{f_m}{4}$ (A, B) and $\frac{f_m}{8}$ (C, D). Considering figures 4, the input-output relations in each of the signal sequencing circuits for the 4th H-bridge cell can be derived from equations (6) and (8) as

$$\begin{bmatrix} g_{a1} \\ g_{b1} \\ g_{c1} \\ g_{d1} \end{bmatrix} = \begin{bmatrix} X_4 & X_3 & X_2 & X_1 \\ X_3 & X_2 & X_1 & X_4 \\ X_2 & X_1 & X_4 & X_3 \\ X_1 & X_4 & X_3 & X_2 \end{bmatrix} \begin{bmatrix} A \bullet C \\ B \bullet C \\ A \bullet D \\ B \bullet D \end{bmatrix} \quad (6)$$

$$\begin{bmatrix} g_{a4} \\ g_{b4} \\ g_{c4} \\ g_{d4} \end{bmatrix} = \begin{bmatrix} Y_4 & Y_3 & Y_2 & Y_1 \\ Y_3 & Y_2 & Y_1 & Y_4 \\ Y_2 & Y_1 & Y_4 & Y_3 \\ Y_1 & Y_4 & Y_3 & Y_2 \end{bmatrix} \begin{bmatrix} A \bullet C \\ B \bullet C \\ A \bullet D \\ B \bullet D \end{bmatrix} \quad (7)$$

Therefore, the switching patterns of the proposed modulation strategy are typified in figure 5.

It can be observed from the proposed switching waveforms in figure 5 that the concept and implementation of proposed switching technique makes the average switching waveform of all the switches in the cascaded H-bridges to be the same. As a result, the four CHB inverter cells operate in a balanced condition with the same power-handling capability and switching losses. Moreover, it is interesting that at the elapse of every fundamental period, the sequence of output voltage synthesis in each of the four cascaded inverter cells is left-shifting; yet the overall cascaded inverter output voltage waveform remains the same. In other words, their respective synthesized output voltage waveforms are dynamically exchanging positions periodically, so that at the elapse of every fundamental period, 4th module becomes the third module, 3rd module becomes the 2nd module, 2nd module becomes the first module and 1st module becomes the 4th module, as seen from the output terminals of the cascaded inverter units.

4. SIMULATION AND EXPERIMENTAL RESULTS

4.1 Simulation Results

Validity of the proposed switching scheme in section 3 is first verified through simulation study carried out in MATLAB/SIMULINK environment. The fundamental frequency switching pulses and their multiples are derived from the base input sinusoidal wave signal. The PWM signals are obtained from the comparison of the reference waveforms of each module with the single-carrier signal. The final sequenced gating pulses are generated from the implementation of the logic AND and OR operations given in equations (6) and (7). For a fundamental and carrier frequencies of 50Hz, and 3kHz, figure 6 shows the simulated waveforms of the output voltages and load current for an RL load. The simulation parameters are: $M_a = 0.9$; $V_S = 200V$, $R = 60\Omega$, $L = 100mH$. Shown in Figure 7 is the power profile of the cascaded inverter system. Obviously, this figure depicts equal power handling capability among the cascaded inverter units. Displayed in Figure 8 is the corresponding harmonic profile of the CHB inverter output voltage.

4.2 Experimental Results

Following the simulation results, a laboratory prototype of the cascaded multilevel PWM inverter is built and implemented using the proposed switching strategy. Table 1 gives the prototype specifications and parameters.

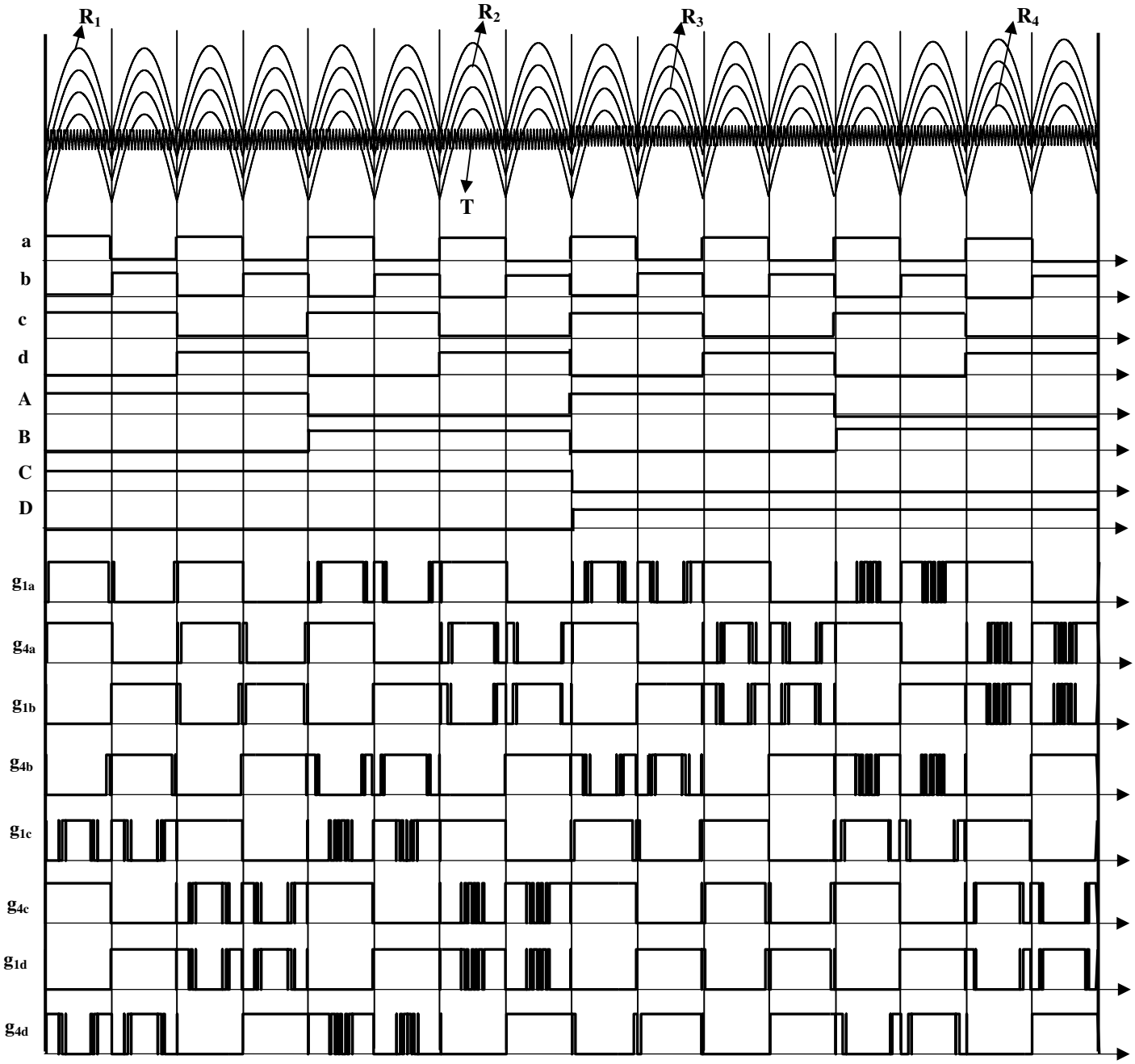


Figure. 5: Switching patterns of the proposed modulation strategy.

Table 1: Prototype specification.

Power switches: IGBT EUPEC BSM 75 GB, 120DLC
R = 60Ω , L = 100mH

The triangular carrier wave at switching frequency of 3KHz and the base sinusoidal reference signal at fundamental frequency of 50Hz were generated using IC TL084. Also, all the base square waves: a, b, c, d, A, B, C and D were generated using 4027 dual J-K flip-flop CMOS IC connected in toggle mode and clocked as earlier indicated in Figure 4. The base switching signal and gating signal sequence generators were implemented using comparators and basic CMOS logic gates. Figure 9 shows experimental waveforms of some gating signals showing equal average switching pulses as earlier predicted. Figure 10 shows the experimental waveforms of modules 1 and 2 individual output voltages; while the overall load voltage and current are shown in Figure 11.

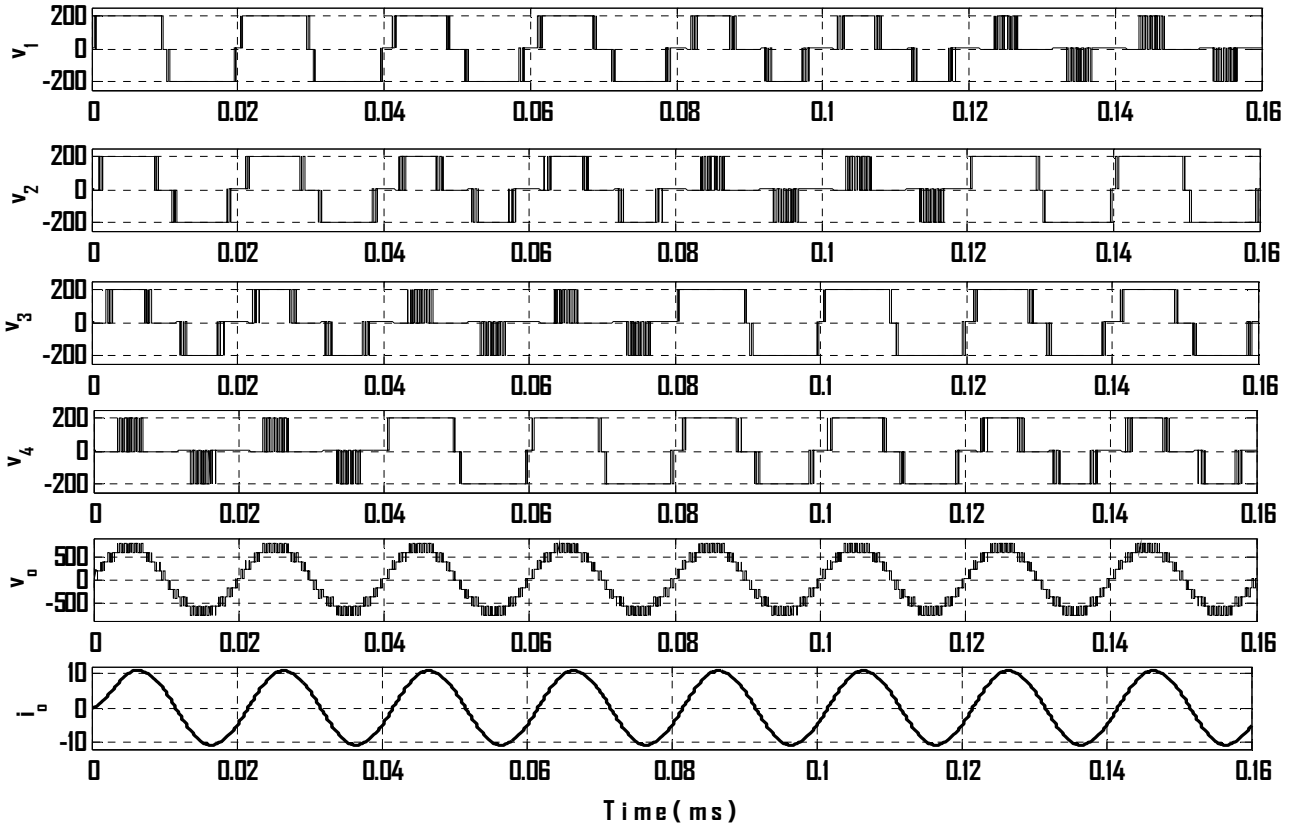


Figure 6: Simulated output voltages and load current

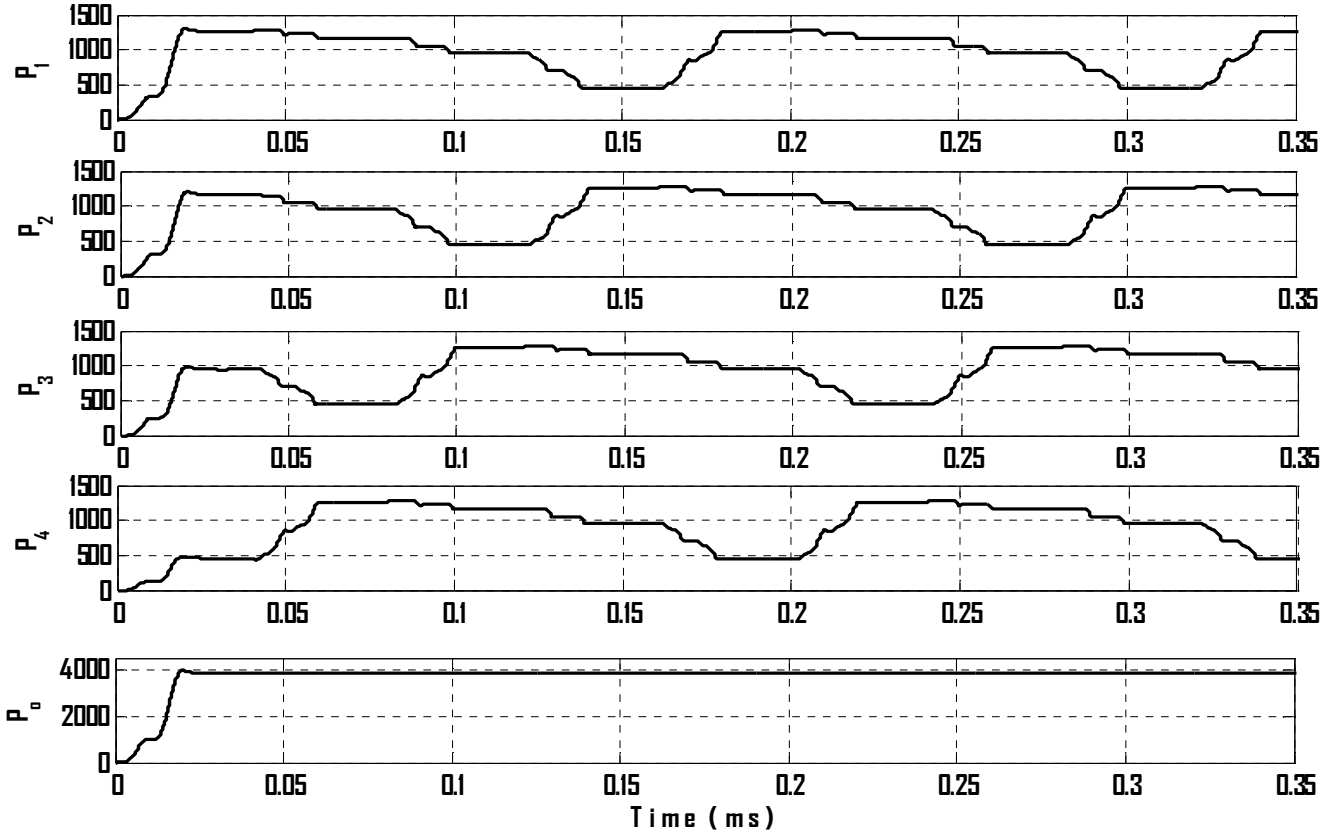


Figure 7: Power profile of CHB inverter under the proposed control strategy

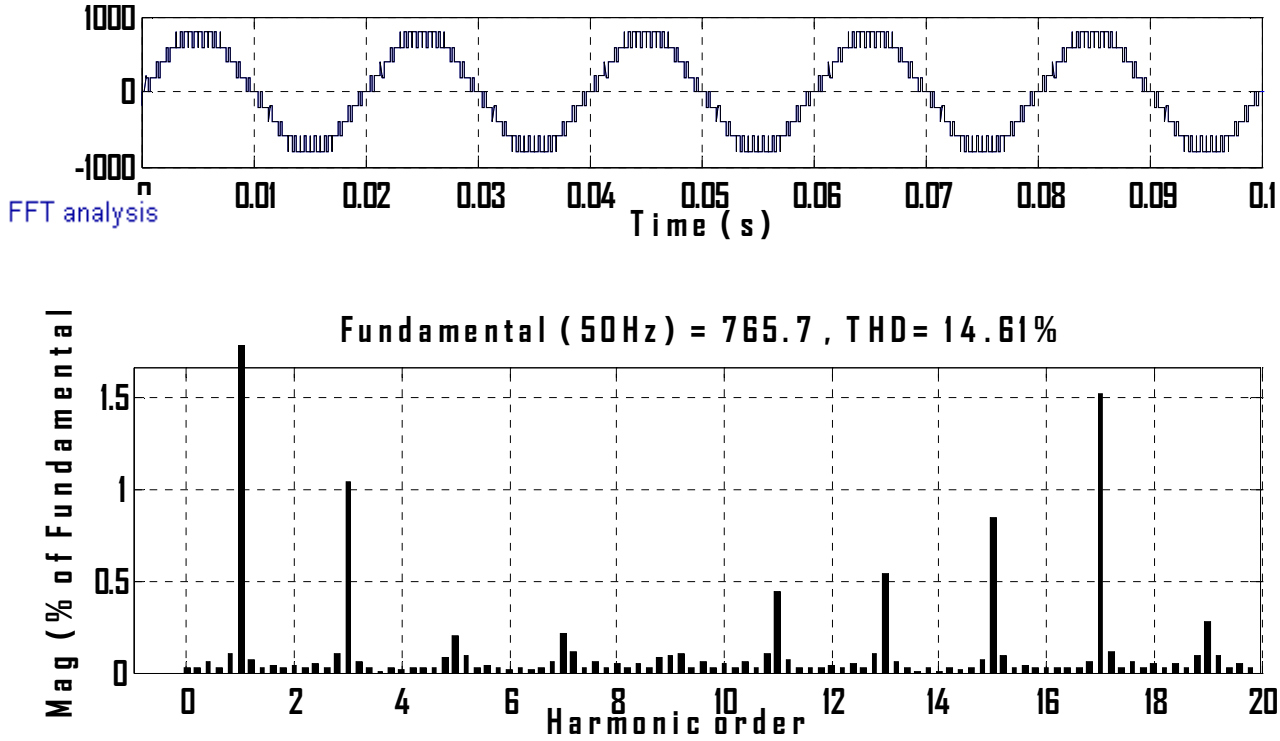


Figure 8: Harmonic profile of the CHB inverter output voltage.

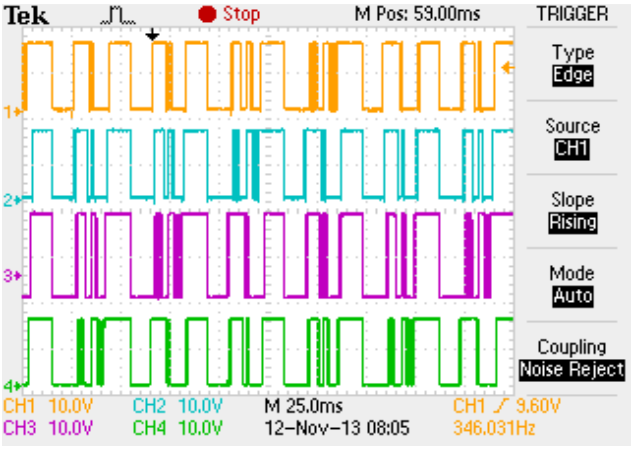


Figure 9: Experimental Gate signals.
CH1: g_{a1}, CH2: g_{b1}, CH3: g_{c1}, CH4: g_{d1}.

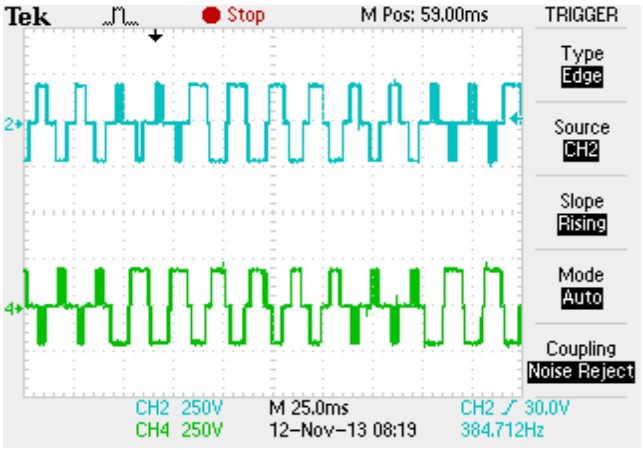
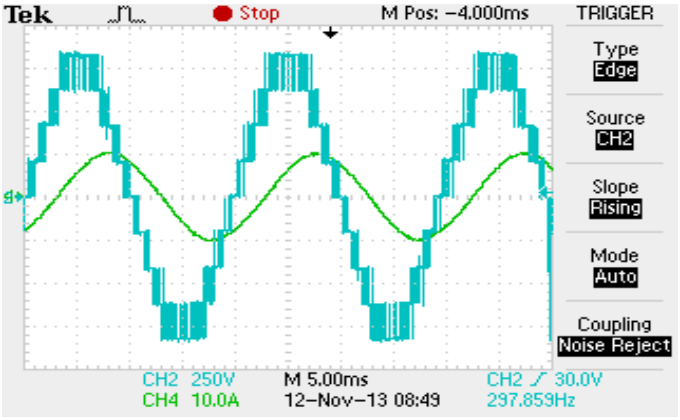


Figure 10: Experimental module voltages.
CH2: v_1, CH4: v_2,



Figuer 11: Experimental waveforms of the output voltage and load current

For the specified R-L load in Table 1, Table 2 gives the measured parameters of the implemented prototype.

Table 2: Parameters of the implemented prototype.

Output voltage (rms): 565.7V
Load current (rms): 7.07A
Measured output power: 4KW

5. CONCLUSION

Presented in this paper is a new switching scheme for CHB multilevel inverter modules. A 4-cell cascaded structure has been used to exemplify the proposed switching technique. It has been shown that the modulation method adopted makes it possible to

generate equal average switching signal patterns in all the constituting power semiconductor switches. Hence, equal switching losses among the power switches have been achieved for CHB inverter units. Accomplished also in this work is the equal power handling capability of all the four CHB inverter cells. With the proposed switching strategy, the overall synthesized output voltage achieved a harmonic profile of 14.61% total harmonic distortion, THD. The performance of the proposed inverter topology has been presented through simulations and experiments on a 4kW rated prototype of the 9-level cascaded multilevel inverter for an R-L load; results have been adequately presented.

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