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EXPERIMENTAL IMPLEMENTATION OF SINGLE-PHASE, THREE-LEVEL, SINUSOIDAL PULSEWIDTH MODULATION (SPWM) VOLTAGE SOURCE INVERTER (VSI) WITH R-L LOAD

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Abstract

The quest to achieve less-distorted dc-ac power conversion has resulted in the proliferation of many multilevel inverter configurations. This paper presents an experimental report of a simplified topology for single-phase, SPWM, three-level voltage source inverter wit R-L load. To keep the power circuit component count to a minimum, the three-level topology simplifies the conventional three-level inverter configuration to that of a full-bridge, two-level inverter, with only one added clamping power switch. Operational principles, with experimental switching functions are given. Laboratory prototypes of the simplified three-level inverter and the conventional full-bridge, two-level inverter were built. Assessment of the 3-level inverter is done by comparing its experimental voltage waveforms and the corresponding FFT analyses with those of the conventional full-bridge, 2-level inverter under the conditions of identical supply dc voltage, switching frequency and loading.

Keywords: SPWM, frequency, single-phase, harmonics

1. Introduction

Simultaneous variation and control of the output voltage and frequency, reduction in the harmonic components in load currents are some of the basic characteristics of PWM inverters. These inherent features have made them to be employed in many industrial applications such as variable speed drives, uninterruptible power supplies and other power conversion systems. However, the reduction of the harmonic components in output currents is still the focus of major interests to mitigate the influence of electro-magnetic interference (EMI) or noise and vibrations. In recent years, many multilevel inverters have been presented, [1]–[5]. The approaches in these technical papers also have a lot of merits such as improved output waveforms, smaller filter size, low EMI and other advantages. Among them, various PWM techniques have been investigated and discussed with their respective characteristics. However, the gate/firing signals to control a particular inverter must be derived before the choice of the switching technique. In general, neutral point clamped PWM three-phase inverter which uses four switching elements in each arm has three level voltage waveforms that result in considerable suppression of the harmonic components when compared with the conventional full-bridge, three-phase, two-level PWM inverter. However, this is not the case with single-phase PWM inverters. In these days, the popular single-phase inverters adopt the full-bridge type using approximate sinusoidal modulation technique. The output voltage in them has two values: zero and positive supply dc voltage levels in the positive half cycle. Hence, the harmonic components of their output voltage are determined by the carrier frequency. Moreover, the harmonic reduction

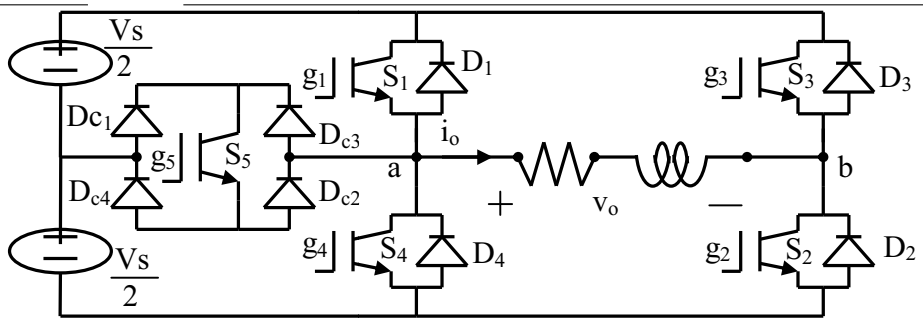


Figure 1: Power circuit of the Single-Phase, Three-level PWM inverter.

in them is limited to a certain degree.

As a solution, [6] presented a single-phase, 3-level, SPWM inverter whose output voltage has three values: zero, half and full supply dc voltage levels in either of the half cycles. This paper thus presents an experimental implementation of this 3-level PWM inverter with an R-L load. Operational principles and experimental switching functions are given.

Assessment of the 3-level inverter is done by comparing its experimental voltage waveforms and the corresponding FFT analyses with those of the conventional full-bridge, 2-level inverter under the conditions of identical supply dc voltage, switching frequency and loading.

2. Configuration and Operational Principles of the Three-Level Inverter

The proposed single-phase, three-level PWM inverter power circuit is shown in figure 1. One switching element and four clamping diodes are added in the conventional full-bridge inverter circuit and are connected to the center-tap of the dc power supply.

The switching patterns which generate the 3-level output voltage from the above circuit are shown in figure 2. Load current and the synthesized output voltage levels according to the switch ON-OFF conditions are shown in table 1, for positive half cycle of the output voltage.

The modes and operational intervals for either half cycle of the output voltage are detailed in [6].

By comparing the rectified sinusoidal signal, V_{ref}, with the two triangular carrier signals, T_1 and T_2, the switching signals g_1 through g_5 of the 3-level inverter are derived from the use of basic logic gates. Equations (1) through (5) give the respective logical operations.

Table 1: Output voltage and current according to the switch ON-OFF conditions.

ON switches	Output voltage	Load current
S_2, D_4	0	$+i_o$
S_4, D_2	0	$-i_o$
D_{c1}, S_5, D_{c2}, S_2	$+V_s/2$	$+i_o$
D_{c3}, S_5, D_{c4}, D_2	$+V_s/2$	$-i_o$
S_1, S_2	$+V_s$	$+i_o$
D_1, D_2	$+V_s$	$-i_o$

$$Ref > 0 = g_2 \tag{1}$$

$$Ref < 0 = g_3 \tag{2}$$

$$[\{(V_{ref} > T_2) \text{ AND } g_2\} \text{ OR } \{(T_1 > V_{ref}) \text{ AND } g_3\}] \tag{3}$$

$$[\{(V_{ref} > T_2) \text{ AND } g_3\} \text{ OR } \{(T_1 > V_{ref}) \text{ AND } g_2\}] \tag{4}$$

$$(T_2 > V_{ref}) \text{ AND } (V_{ref} > T_1) \tag{5}$$

3. Experimental Results

The results in [6] are verified experimentally and reported herein. The prototype setups of the 3- and 2- level inverters are shown in figure 3. The logical operations in equations (1) through (5) are implemented using basic CMOS IC gates: 4081, 4071, 4049 and TL084 quad comparator. Specifications of the power circuit components are given in table II. Experimental waveforms of the firing pulses to the power switches are shown in figures 4 and 5.

Figures 6 through 8 show the experimental waveforms of the output voltage and current as the modulation index is varied from 0.4 to 1.2, for

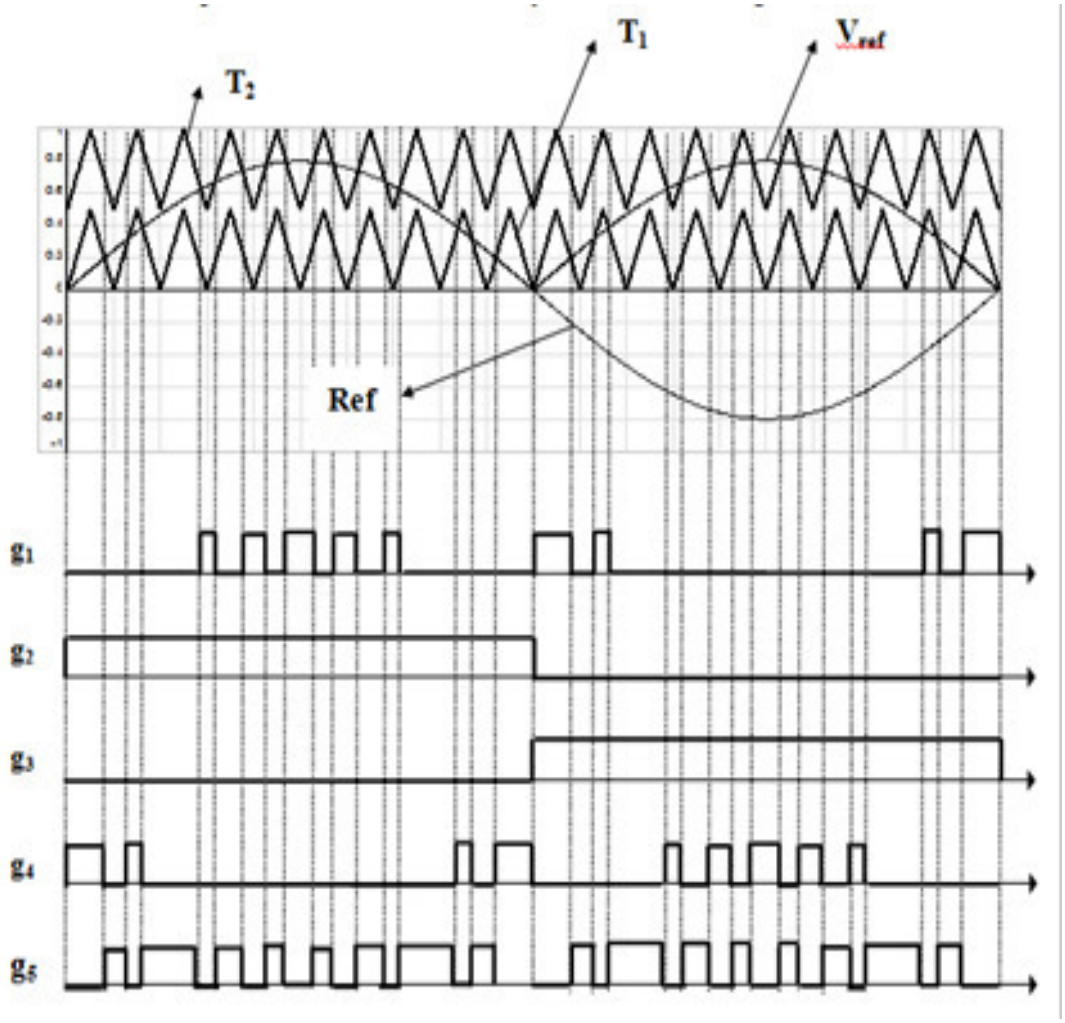


Figure 2: Switching pattern of the proposed single-phase, three-level PWM inverter.

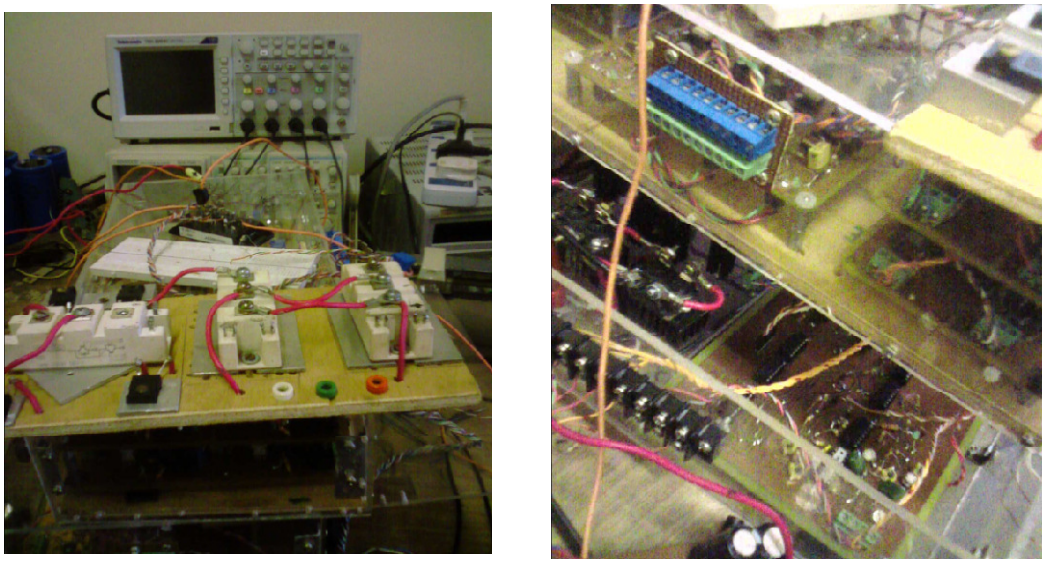


Figure 3: Prototype setup. (a) Power circuits for both inverters. (b) Logic and Driver circuits.

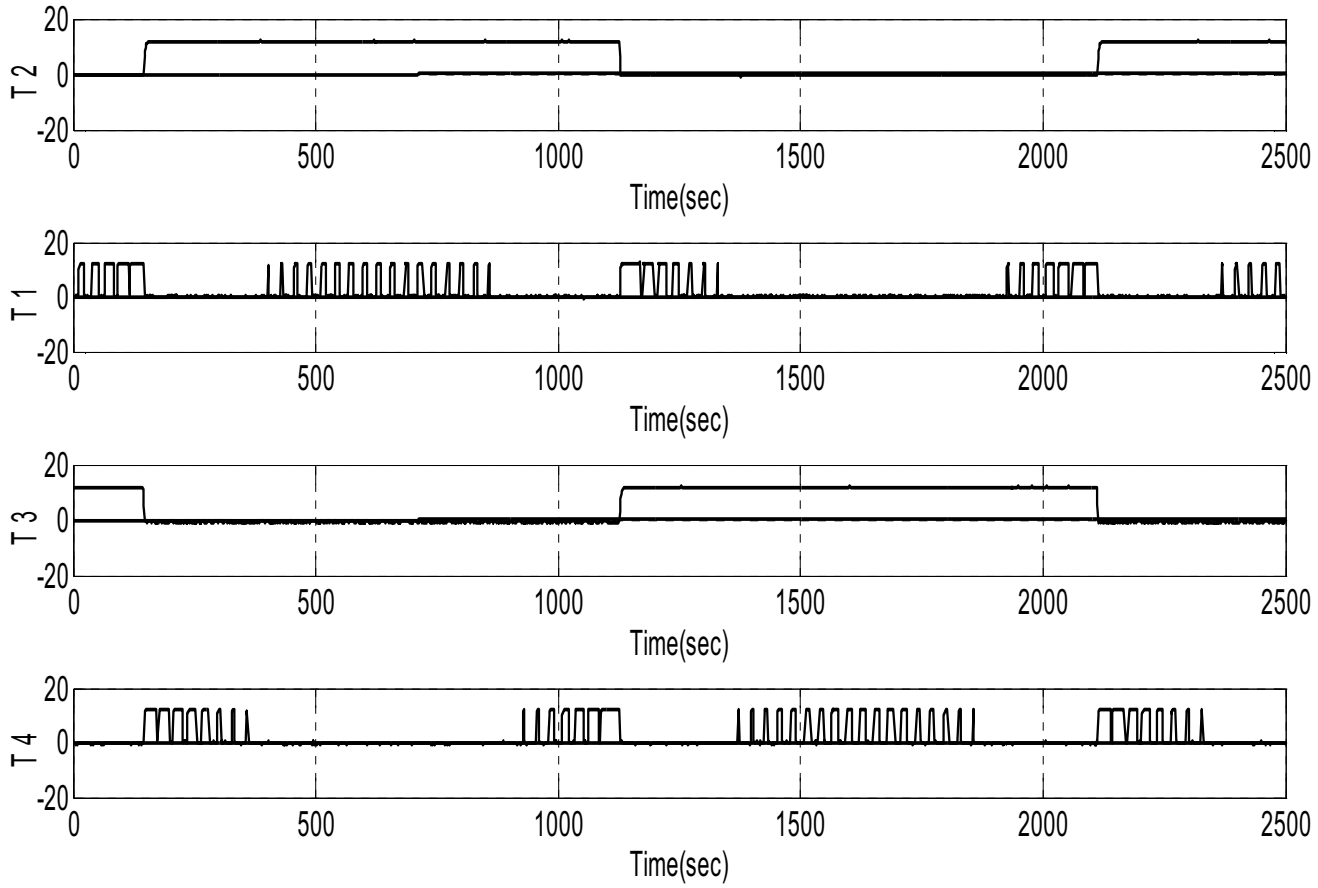


Figure 4: Experimental waveforms of the gating signals of the 3-level inverter. (a), T_2, T_1, T_3 and T_4.

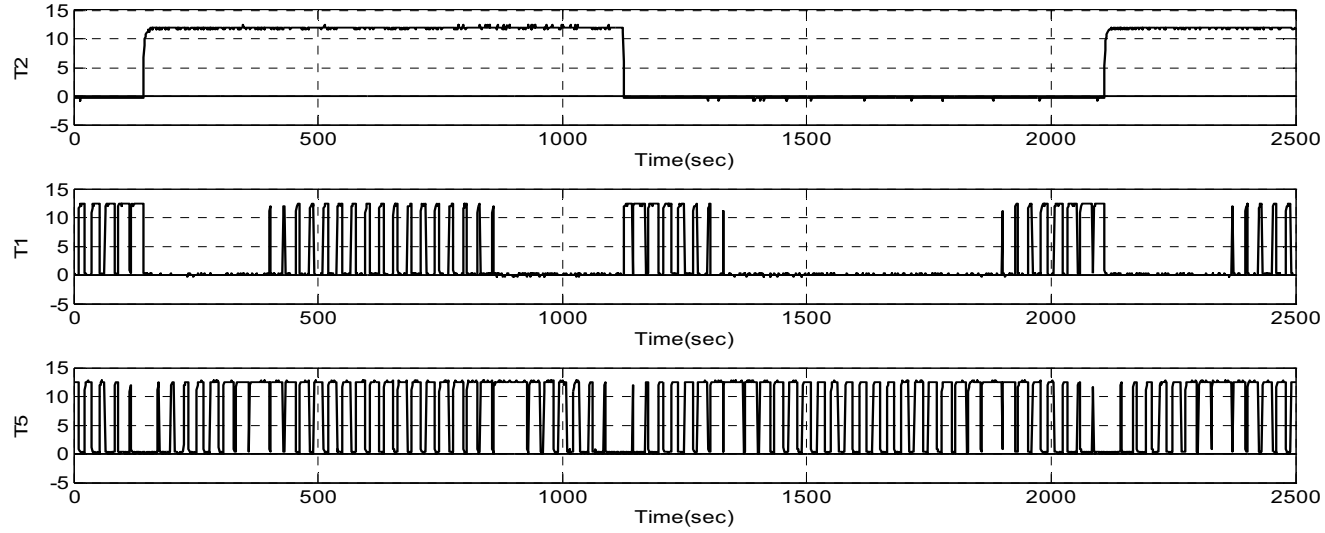


Figure 5: Experimental waveforms of the gating signals. (a) T_2, T_1 and T_5.

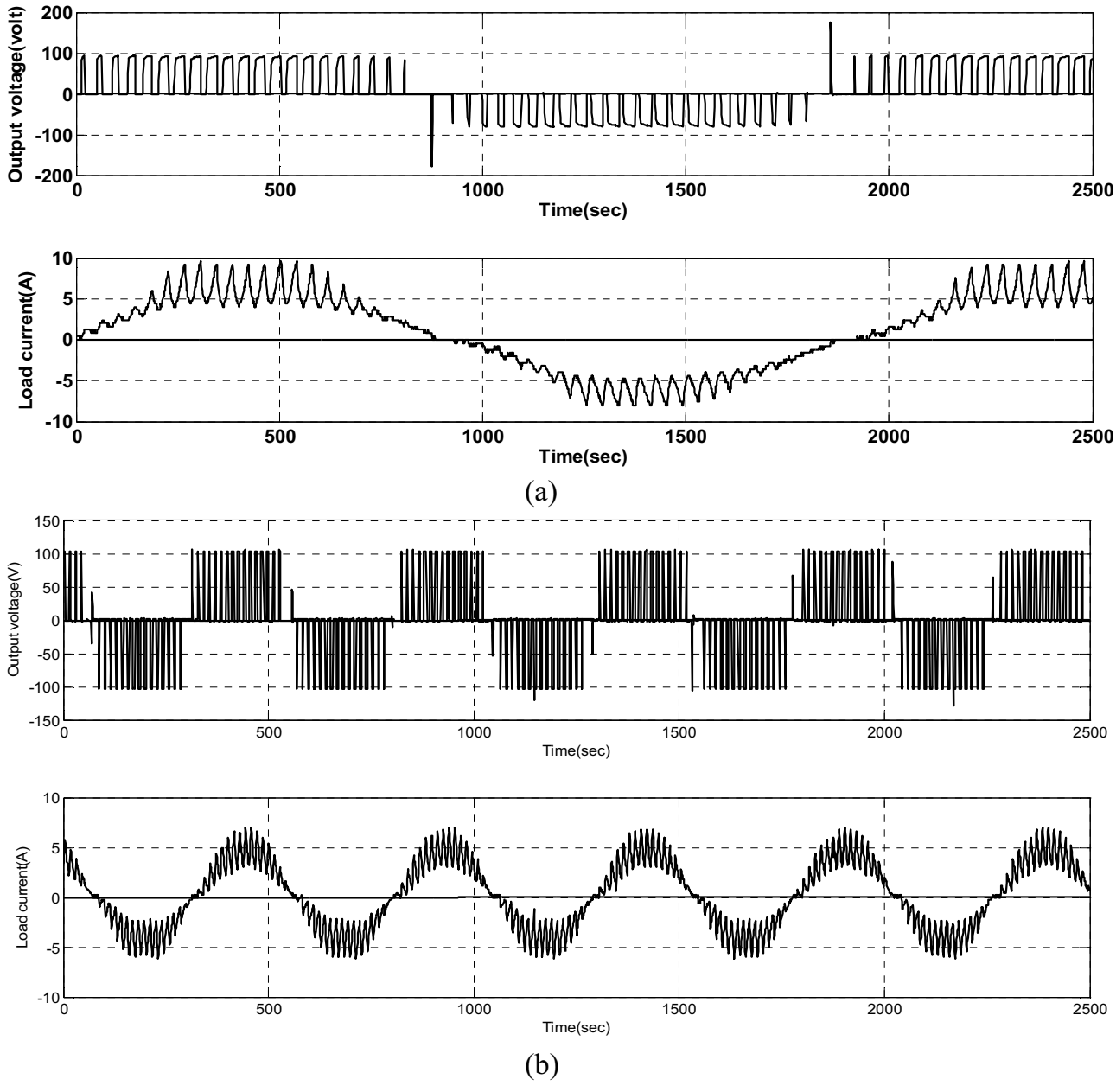


Figure 6: Experimental output voltage and load current for modulation index of 0.4.(a) Simplified three-level inverter. (b) Conventional full-bridge, 2-level inverter.

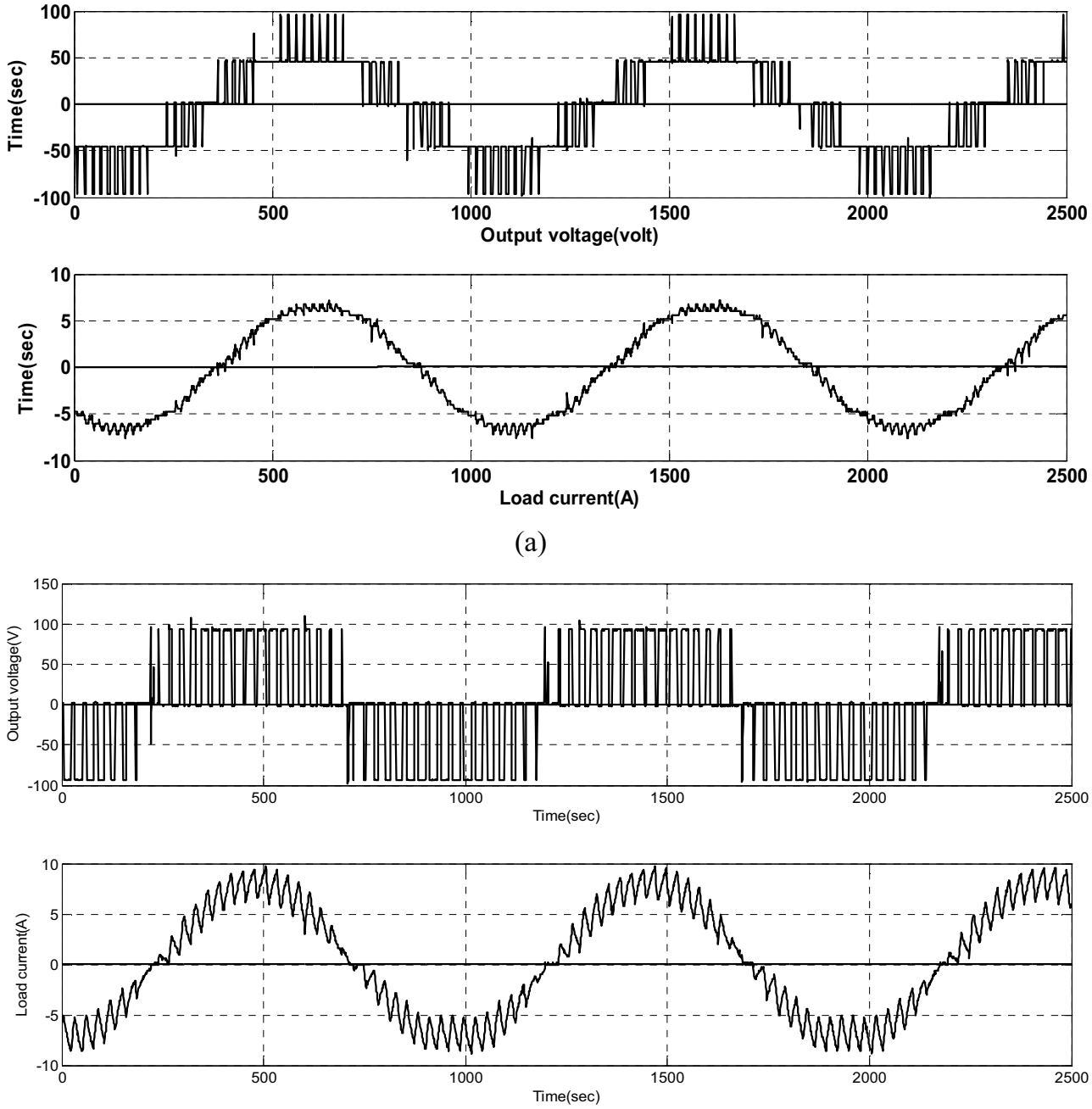
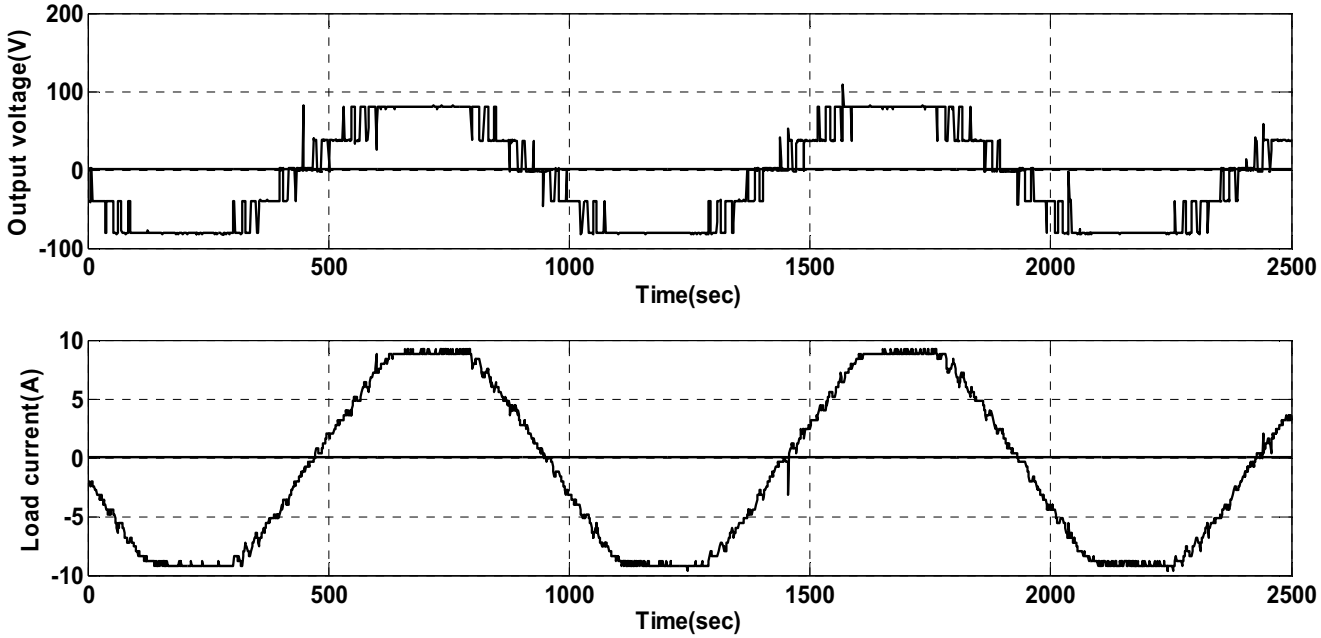
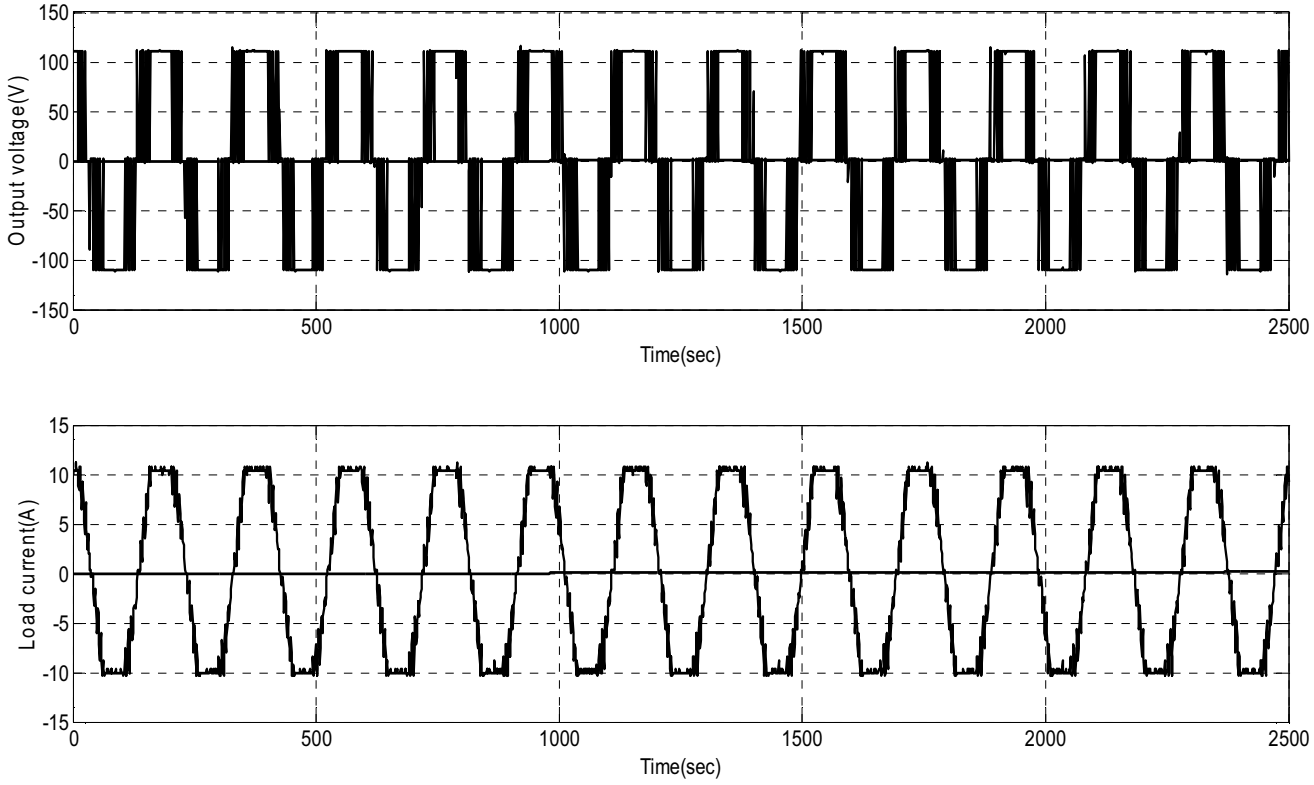


Figure 7: Experimental output voltage and load current for modulation index of 0.8.(a) Simplified three-level inverter. (b) Conventional full-bridge, 2-level inverter.



(a)



(b)

Figure 8: Experimental output voltage and load current for modulation index of 1.2. (a) Simplified three-level inverter. (b) Conventional full-bridge, 2-level inverter.

Figure 9: Comparison of the harmonic profile of the output voltages of the two inverters. (a) 3-level inverter, $Ma = 0.4$. (b) 2-level inverter, $Ma = 0.4$. (c) 3-level inverter, $Ma = 0.8$. (d) 2-level inverter, $Ma = 0.8$. (e) 3-level inverter, $Ma = 1.2$. (f) 2-level inverter, $Ma = 1.2$.

Table 2: Output voltage and current according to the switch ON-OFF conditions.

Component	Specification
$S_1 - S_5$	IGBT IRG4PC40UDPBF, $V_C E = 600$, $I_C = 20$A
$D_{c1} - D_{c4}$	RHRP30120 $V_{RR} = 1200$V, $I = 30$A
L	4mH
R	25Ω
Switching frequency	5kHz

the conventional single-phase, 2-level and simplified 3-level inverters.

To show that the simplified 3-level inverter topology has advantage over the conventional 2-level PWM inverter in terms of enhanced harmonic profile, FFT analyses were carried out on each of the output voltage waveforms in figures 5 through 7. Figure 9 shows a comparison of the harmonic profile for the two inverter configurations.

With 0.4 modulation index, both inverters have nearly similar harmonic components distribution, differing in their quantities because of their different pulse widths and amplitude of the used input dc source. With 0.8 modulation index, the harmonic components of the 3-level inverter are really smaller than those of the conventional 2-level inverter. In the over-modulation region, the output voltages of both inverters contain more harmonics in the lower order.

4. Conclusions

This paper has presented an experimental report on a simplified single-phase, three-level, SPWM inverter that reduced the harmonic components of the output voltage and load current inherent in the conventional 2-level, single-phase inverter. The operational principles and experimental switching functions were given. Analyses of the output voltage waveforms from the laboratory prototypes of the aforementioned inverter topologies showed a better frequency spectrum.

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