NEW TOPOLOGY FOR SINGLE-PHASE, THREE-LEVEL, SPWM VSI WITH LC FILTER

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Abstract

Multilevel inverters that provide more than two levels of voltage to achieve less distorted dc-ac conversion have attracted many contributors. This paper presents a new simplified topology for single-phase, sinusoidal pulse width modulated (SPWM) three-level SPWM voltage source inverter (VSI) with LC filter. To keep the power circuit component count to a minimum, the proposed three-level topology simplifies the conventional three-level inverter configuration to that of a full-bridge, two-level inverter, with only one added auxiliary power switch. Operational principles, with switching functions are analyzed. The performance characteristics of the proposed inverter are predicted using simulation process in simplorer schematic environment. Assessment of the proposed inverter is done by comparing it with the conventional single-phase, two and three level SPWM inverter under the conditions of identical supply dc voltage, switching frequency and loading.

Keywords: SPWM inverter, Frequency, single-phase, Harmonics

1. Introduction

Simultaneous variation and control of the output voltage and frequency, reduction in the harmonic components in load currents are some of the basic characteristics of PWM inverters. These inherent features have made them to be employed in many industrial applications such as variable speed drives, uninterruptible power supplies and other power conversion systems. However, the reduction of the harmonic components in output currents is still the focus of major interests to mitigate the influence of electro-magnetic interference or noise and vibrations. In recent years, many multilevel inverters have been presented, [1] [5]. The approaches in these technical papers also have a lot of merits such as improved output waveforms, smaller filter size, low EMI and other advantages. Among them, various PWM techniques have been investigated and discussed with their respective characteristics. However, the gate/firing signals to control a particular inverter must be derived before the choice of the switching technique. In general, neutral point clamped PWM three-phase inverter which uses four switching elements in each arm has three level voltage waveforms that result in considerable suppression of the harmonic components when compared with the conventional full-bridge, three-phase, two-

level PWM inverter. However, this is not the case with single-phase PWM inverters. In these days, the popular single-phase inverters adopt the full-bridge type using approximate sinusoidal modulation technique. The output voltage in them has two values: zero and positive supply dc voltage levels in the positive half cycle. Hence, the harmonic components of their output voltage are determined by the carrier frequency. Moreover, the harmonic reduction in them is limited to a certain degree.

As a solution, this paper presents a single-phase, three-level PWM inverter whose output voltage has three values: zero, half and full supply dc voltage levels in the positive half cycle. The proposed inverter can reduce the harmonic components compared with that of the conventional full-bridge, two-level PWM inverter under the condition of identical supply dc voltage, switching frequency and loading. Operational principles and switching functions are analysed. Simulation results are presented to verify the validity of the proposed inverter.

2. Configuration and Operational Principles of the Proposed Inverter.

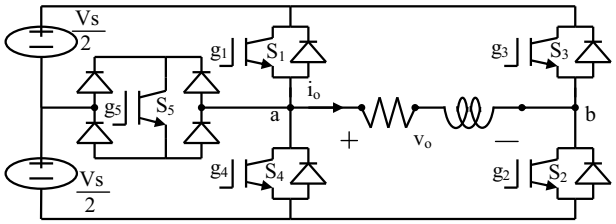

Figure 1: Power circuit of the proposed Single-Phase, Three-level PWM inverter.

The proposed single-phase, three-level PWM inverter power circuit is shown in figure 1. One switching element and four clamping diodes are added in the conventional full-bridge inverter circuit and are connected to the center-tap of the dc power supply. Proper gating control of the auxiliary power switch can generate half level of the dc supply voltage. The operation of the proposed inverter can be divided into ten switching states as illustrated in Figure 2.

Table 1: Output voltage according to the switch ON-OFF conditions.

ON switches	Node a voltage (v_a)	Node b voltage (v_b)	Output voltage ($v_{ab} = vo$)
S_1, S_4	V_s	0	$+V_s$
S_5, $S4$	$V_s/2$	0	$+V_s/2$
S_2, S_4 (S_1, S_3)	0	0	0
S_2, S_5	0	$V_s/2$	$-V_s/2$
S_2, S_3	0	V_s	$-V_s$

Operational states of the conventional two-level inverter are shown in figure 2(i), (ii), (v), (vi), (vii) and (viii) in sequence; and additional states in the proposed inverter synthesizing half level of dc bus voltage are shown in figure 2(iii), (iv), (ix) and (x). The additional switch, s5 must be properly triggered considering the direction of the load current, io. The switching patterns adopted in the proposed inverter are illustrated in Figure 3; and the output voltage levels according to the switch on-off conditions are shown in Table 1.

Basic principle of the proposed switching strategy is to generate triggering signals by comparing the reference signal with two disposed carrier waves having the same frequency and in phase, but different offset voltages. If the required output voltage for a certain load can be produced using only the half of the dc bus voltage, only the lower carrier wave is compared with reference signal. Power switches S2, S3 and S5 are used to generate the output voltage. In this case, the modulation index is equal or less than 0.5 and the behaviour of the proposed inverter is similar to that of conventional full-bridge, two-

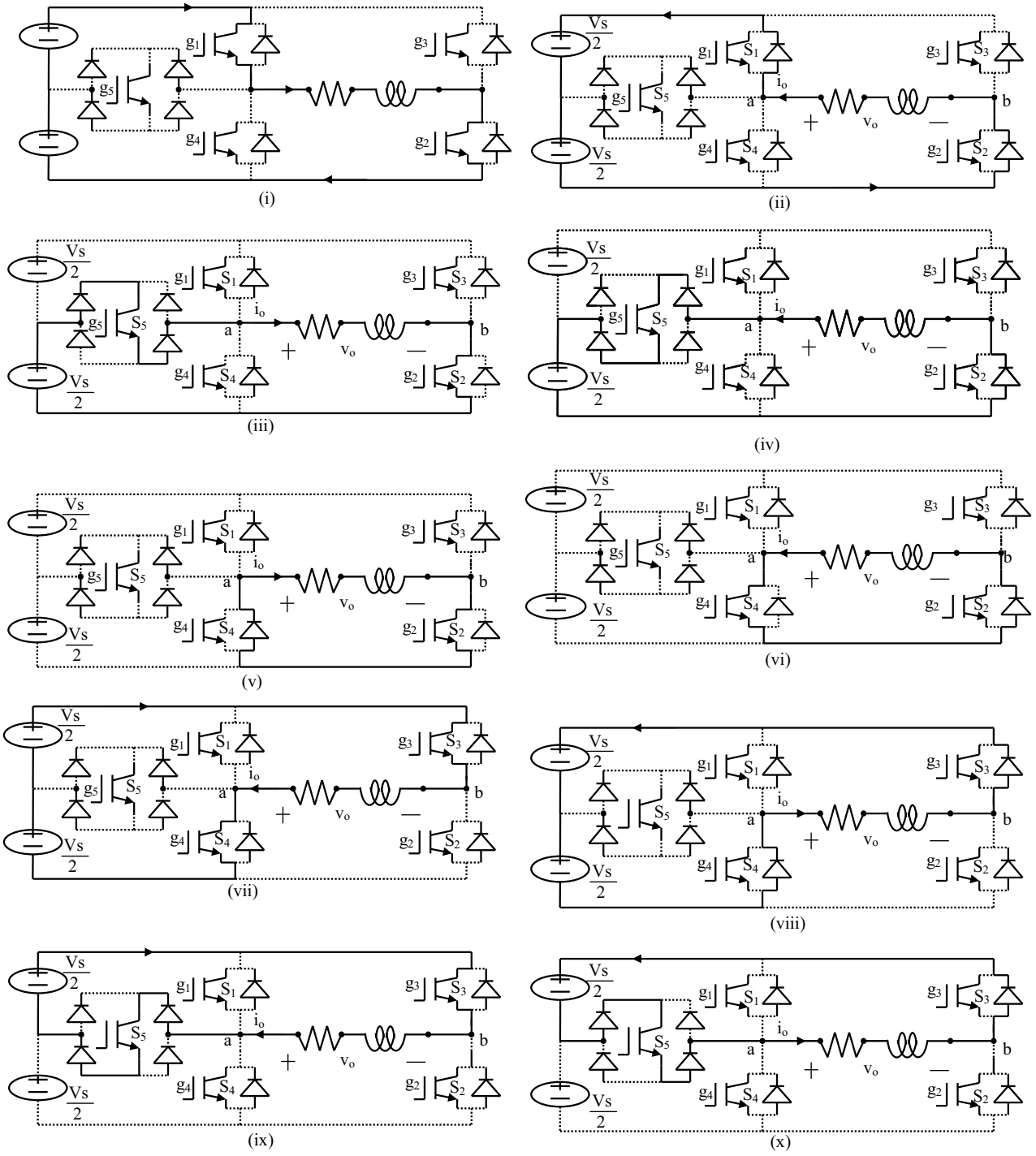

Figure 2: Operation states according to the switch on-off conditions and the direction of load current. (i) state 1: $v_o = v_s,\ i_o + ve$. (ii) state 2: $v_o = v_s,\ i_o - ve$. (iii) state 3: $v_o = v_s/2,\ i_o + ve$. (iv) state 4: $v_o = v_s/2,\ i_o - ve$. (v) state 5: $v_o = 0,\ i_o + ve$. (vi) state 6: $v_o = 0,\ i_o - ve$. (vii) state 7: $v_o = -v_s,\ i_o - ve$. (viii) state 8: $v_o = -v_s,\ i_o + ve$. (ix) state 9: $v_o = -v_s/2,\ i_o - ve$. (x) state 10: $v_o = -v_s/2,\ i_o + ve$.

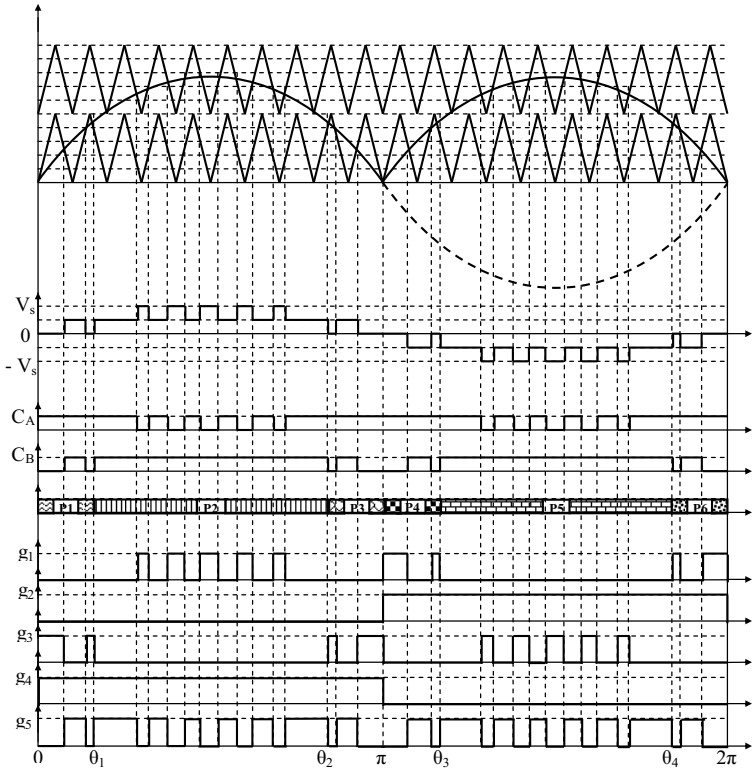

Figure 3: Switching pattern of the proposed single-phase, three-level PWM inverter.

level PWM inverter. This is just the first operational mode. On the other hand, if the modulation index is increased beyond 0.5, it comes into the second mode, and all the power switches are employed to generate the three-level output voltage. In this mode, the switching functions are produced by the comparison of the reference modulating signal with the upper and lower triangular carrier waves. Depending on the amplitude of the reference signal vref, the operational interval of each mode varies within a certain period. The modes are separated as

$$\begin{aligned} &\text{Mode A} : 0 < \omega t\theta_1, \theta_2 < \omega t\pi; \\ &\text{Mode B} : \theta_1 < \omega t \leq \theta_2 \\ &\text{Mode C} : \pi < \omega t \leq \theta_3, \theta_4 < \omega t \leq 2\pi; \\ &\text{Mode D} : \theta_3 < \omega t \leq \theta_4 \end{aligned} \tag{1}$$

The phase angles θ_1 through θ_4 depend on the Amplitude modulation index M_a. The modulation index of the proposed three-level inverter is defined as [6]

$$M_a = \frac{A_m}{2A_c} \tag{2}$$

where A_m is the peak value of the reference signal and A_c is the peak-to-peak value of the carrier signal. When the modulation index is less than 0.5, the phase angle displacement is equal to

$$\theta_1 = \theta_2 = \frac{\pi}{2}, \quad \theta_3 = \theta_4 = \frac{3\pi}{2} \tag{3}$$

However, if the modulation index is above 0.5, the phase angle displacement is determined by

$$\begin{aligned} &\theta_1 = \sin^{-1}\left(\frac{A_c}{A_m}\right), \quad \theta_2 = \pi - \theta_1, \\ &\theta_3 = \pi + \theta_1, \quad \theta_4 = 2\pi - \theta_1 \end{aligned} \tag{4}$$

By comparing the reference signal with the respective carrier signals, the control signals

C_A and C_B are generated as shown in figure 3. Consequently, the switching signals g_1 through g_5 of the proposed inverter are derived from the use of basic logic gates on the signals C_A, C_B and the phase angle displacements; equation (5) gives the respective logical operations.

$$\begin{aligned} g_1 &= \overline{C_A}P_2 + \overline{C_B}P_4 + \overline{C_B}P_6; \\ g_2 &= P_4 + P_5 + P_6; \\ g_3 &= \overline{C_B}P_2 + \overline{C_B}P_3 + \overline{C_A}P_5; \\ g_4 &= P_1 + P_2 + P_3; \\ g_5 &= C_BP_1 + C_AC_BP_2 + C_BP_3 \\ &\quad + C_BP_4 + C_AC_BP_5 + C_BP_6 \end{aligned} \tag{5}$$

From the two disposed carrier waves and output voltage in figure 3, the analysis of the harmonic components in the proposed inverter can be performed. The output voltage produced by the comparison of the reference signal and the two carrier waves can be expressed as

$$V_o(\theta) = A_o + \sum_{n=1}^{\infty}(A_n \cos n\theta + B_n \sin n\theta) \tag{6}$$

If there are P pulses per a quarter period, and it is an odd number, the coefficients Bn and A0 would be zero. Thus, equation (6) simplifies to

$$V_o(\theta) = A_o + \sum_{n=1,3,5,\ldots}^{\infty}(A_n \cos n\theta) \tag{7}$$

where m is a pulse number.

The Fourier series coefficients of the conventional single-phase, full-bridge, sinusoidal PWM inverter is given by

$$A_n = \frac{2V_s}{n\pi}\sum_{m=1}^{P}\{(-1)^m \sin(n\alpha_m)\} \tag{8}$$

3. Performance Estimation of the Proposed Inverter

Reduction in the harmonic components of the output voltage synthesized by an inverter system is highly needed as it alleviates the output current ripples; as well as minimizes the size of the output filter. Simulation study is carried out on the proposed single-phase, three-level inverter to evaluate its characteristic performance. The simulation is done in the SIMPLORER schematic environment.

Figure 4(i) through 4(viii) show the simulated waveforms of the output voltage and load current as the modulation index is varied from 0.4 to 1.4 in steps of 0.4 for the conventional single-phase, two-level and the proposed three-level inverters.

When the modulation index equal or less than 0.5, the behaviour of the proposed inverter is similar to that of the conventional full-bridge, two-level inverter which is controlled by a sinusoidal PWM. However, if the modulation index is greater than 0.5, the behaviour of the two inverter models become different. The proposed three-level inverter comes into the second mode, and the conventional two-level only changes its pulse-width. To increase further the amplitude of the fundamental frequency component in the output voltage, the modulation index may be increased beyond unity for both inverters. In this case, the output voltage waveforms degenerate from a pulse-width modulated waveform into a nearly square wave as shown in figure 4(vii) and (viii).

Figure 5 shows a comparison of each harmonic component distribution for the conventional two-level and the proposed three-level inverters. They are compared up to 100 order harmonic components according to the variation of the modulation index. With modulation index of 0.4, both inverters have nearly similar harmonic components distribu-

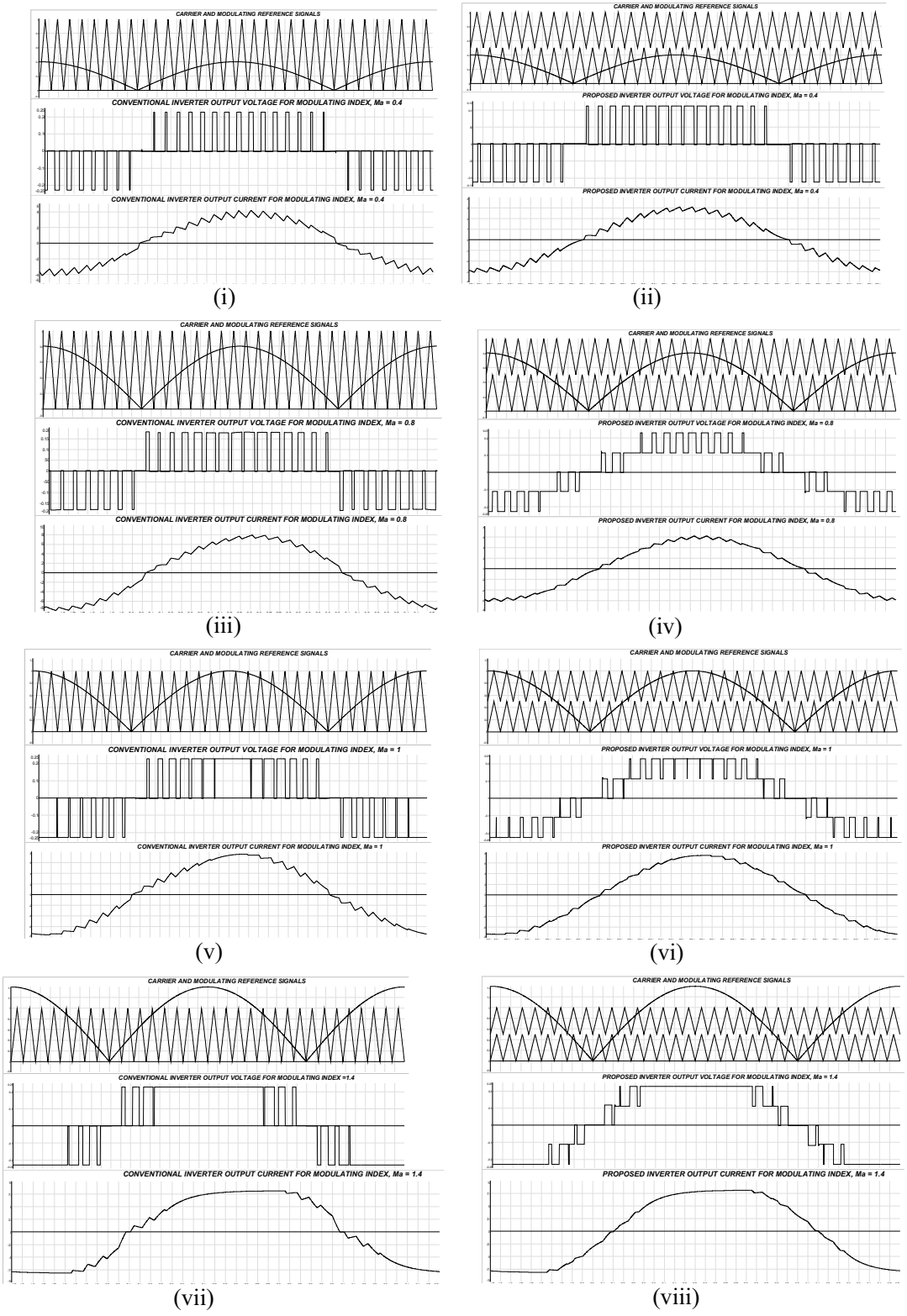

Figure 4: Simulated output voltage and load current with modulation index, Ma. (i) Conventional, Ma = 0.4. (ii) Proposed, Ma = 0.4. (iii) Conventional, Ma = 0.8. (iv) Proposed, Ma = 0.8. (v) Conventional, Ma = 1. (vi) Proposed, Ma = 1. (vii) Conventional, Ma = 1.4. (viii) Proposed, Ma = 1.4.

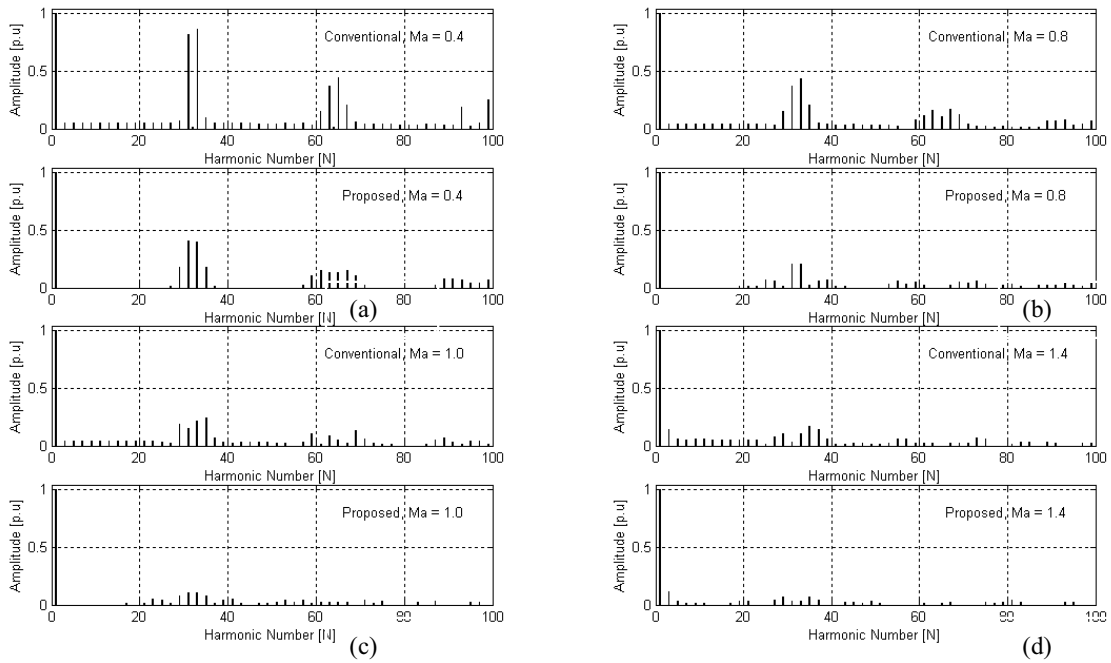

Figure 5: Comparison of each harmonic component. (a) Ma = 0.4. (b) Ma = 0.8. (c) Ma = 1. (d) Ma = 1.4.

tion, differing in their quantities because of their different pulse widths and amplitude of the used input dc source. In the range Ma 1.0, the harmonic components of the proposed inverter are smaller than those of the conventional two-level inverter. However, in the over-modulation region, the output voltages of both inverters contain more harmonics in the lower order. Beside, the harmonics with dominant amplitudes in the linear range Ma 1.0 are recessive during over-modulation as shown in figure 5(d). It can also be inferred from the displayed spectra that the amplitude of the fundamental frequency component does not vary linearly with the amplitude modulation ratio, Ma. Figure 6 shows a comparison of the total harmonic distortion, THD of the output current for both inverters. From this graph, it is clear that the THD of the proposed inverter has lower values than those of the conventional two-level inverter.

Table 2: A Comparison of the 3-level, diode-clamped and the proposed inverters.

	Diode clamped	Proposed
Main switches	$2(m+1)$	$2m-1$
Main diodes	$3(m+1)$	$2(m+1)$
Gate-Amp	$2(m+1)$	$2m-1$
DC-link	Bulk Capacitor	Bulk Capacitor

Furthermore, the power circuit of the proposed inverter is compared with that of conventional single-phase, three-level, diode-clamped inverter shown in Figure 7.

The comparison between the diode-clamped and the proposed three-level, single-phase inverters is listed in Table 2; where m is the number of output voltage levels per half cy-

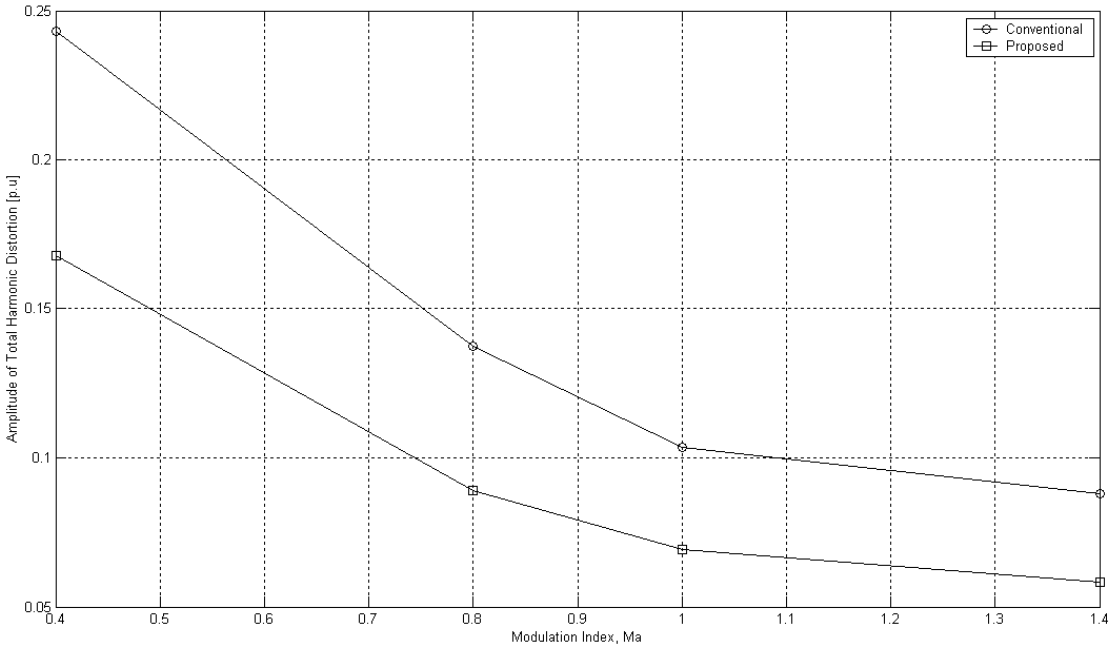

Figure 6: Total harmonic distortion according to the variation of the modulation index.

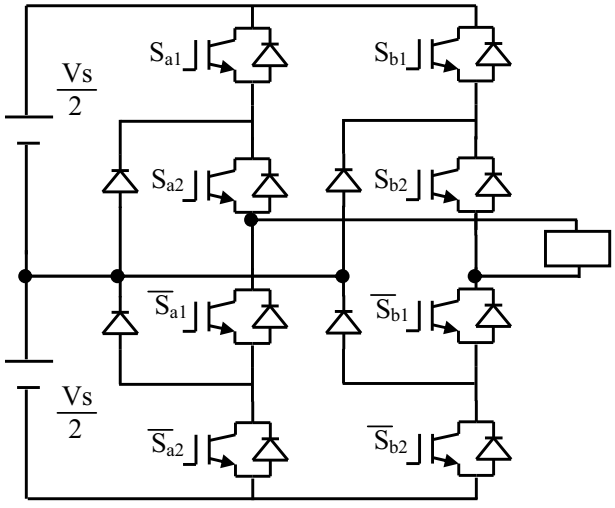

Figure 7: Conventional single-phase, Three-level Diode-clamped Voltage source inverter.

cle: m = 3. From Table 2, the most outstanding advantage of the proposed inverter is the reduced number of power switches, and of course their corresponding gate-amp. But both inverter topologies need a large value of capacitor to prevent the asymmetry of dc-link voltages.

4. Conclusion

This paper has presented a single-phase, three-level PWM inverter that drastically reduced the harmonic components of output voltage and load current inherent in the conventional two-level, single-phase inverter. The operational principles and switching functions have been analyzed. Reduction in the number of power circuit, power semiconductor switching devices associated with the proposed inverter topology when compared with the conventional single-phase, three-level, diode-clamped VSI has been shown. Simulation re-

sults show that the THD of the proposed inverter is considerably enhanced.

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