A GENERALIZED APPROACH TO ANALYSING A CLASS OF PASSIVELY SOFT-SWITCHED PWM DC-DC CONVERTERS

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ABSTRACT

In this paper, a generalised approach to the analysis of a class of passively soft-switched PWM DC-DC converters is presented. The circuit cell that gives this class of converters its passively soft-switched characteristics is first introduced. The use of this circuit cell to transform the basic hard switched converters (buck, boost, bucklboost, Cuk's, Sepic and Zeta) into their varied passively soft-switched PWM topologies is illustratively presented. A generalised analysis representative of all the soft-switched converter types in the class is carried out.

1. INTRODUCTION

The switching losses of the conventional hard-switched dc to dc converter increase with increase in operating frequency. These switching losses include the active switch current and voltage overlap loss during the switching interval, the capacitance losses during the active switch turn on and diode reverse recovery loss during the diode turn off. But operation at high frequency has the advantage of resulting in considerable reduction of the size and weight of circuit reactive components for a given power output. Some proposals have been made to minimise or eliminate these losses at high frequency. The earlier proposals to achieve this are mainly various forms of the frequency or pulsewidth modulated (FM or PWM) quasi- resonant converters (unclamped or clamped) that use zero current and/or zero voltage switching to minimise switching loss [1 -11]. But each of these converters suffers from one or more of the disadvantages of high current and voltage stresses, the presence of more than one active switch, active switch capacitive turn on loss, elaborate cross zero detection circuit, difficulties and adverse effects of FM control, converter freewheeling diode turn off loss and/or increased number of reactive components. Several topologies [12-19] of the soft-switched PWM converter have been proposed to minimise or eliminate most of these disadvantages. Each of these proposed PWM converters is either actively [12-16] or passively [17-19] soft switched and, in most cases [12-14 & 17-18], the soft switching circuit cell is applicable to only one dc-dc single stage converter type. The actively soft-switched PWM converter has two or more active switches and therefore relatively elaborate control circuitry. On the other hand, the passively soft- switched single stage converter has only one active switch and much simpler control requirement. Reference 19 reports some passively soft switching circuit cells that provide zero current (ZC) turn on and zero voltage (ZV) turn off of the active switch and ZC plus ZV turn off and ZV turn on of the main converter free wheeling diode. The work in this paper is an extension to show the versatility of one of the proposed circuit cells (in reference 19) which provides soft switching for all the basic single stage dc-dc converter types at minimum voltage and current stress to the circuit components. The versatility is shown by using the circuit cell to configure 12 single stage converter topologies and then giving one generalised procedure that enables the design and the performance determination of the converters.

2. THE CIRCUIT CELL AND THE SOFT - SWITCHED CONVERTER TOPOLOGIES

The circuit cell used in realising the passively soft-switched PWM converter is shown in Fig. 1 as a three terminal device. The use of Type A or Type B of the cell depends on the basic converter configuration. In the cell topology, D is the free wheeling diode that forms part of the basic converter, L_r C_r are the resonant inductor and capacitor respectively. D_{s1}, D_{s2} and D_{s3} are the snubber diodes while C_s is the snubber capacitor.

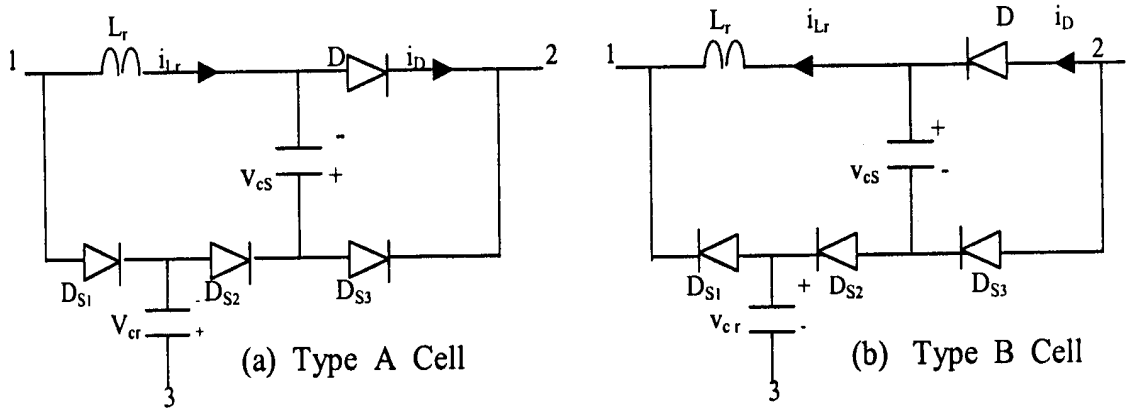
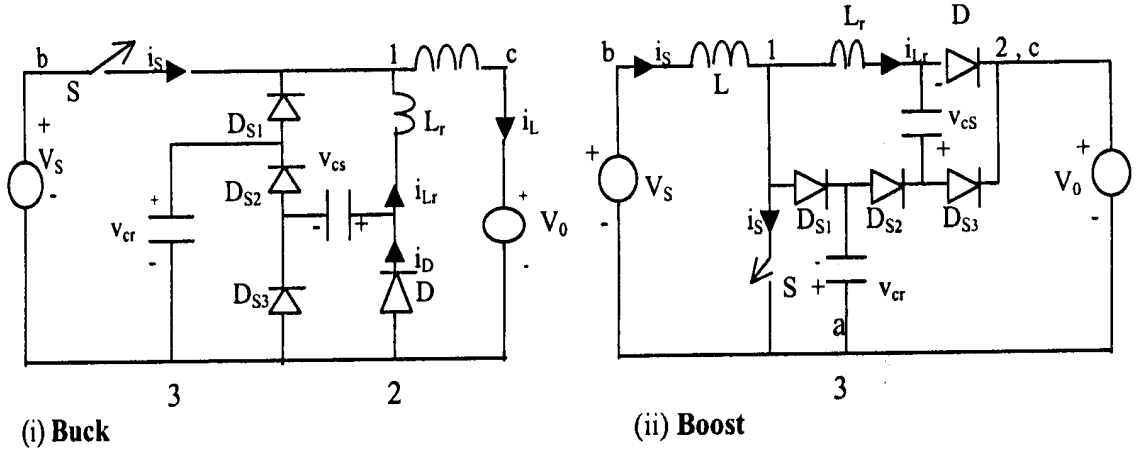
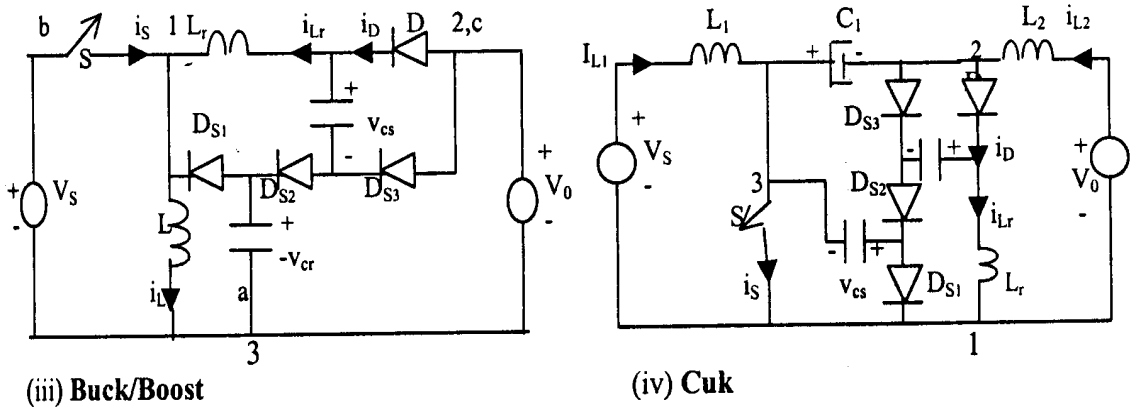


Fig. 1: Circuit Cells for realising the soft-switched Converters

Fig. 2 shows the cell connection in the basic conventional dc-dc converters (buck, boost, buck/boost, Cuk's, sepic and zeta converters) to make these converters to be passively soft switched. For each of the first three converters (the buck, boost and buck/boost), there are three possible connection points (a, b and c) for terminal 3 of the circuit cell but for each of the remaining three up/down converters, only one connection point for terminal 3 is possible.





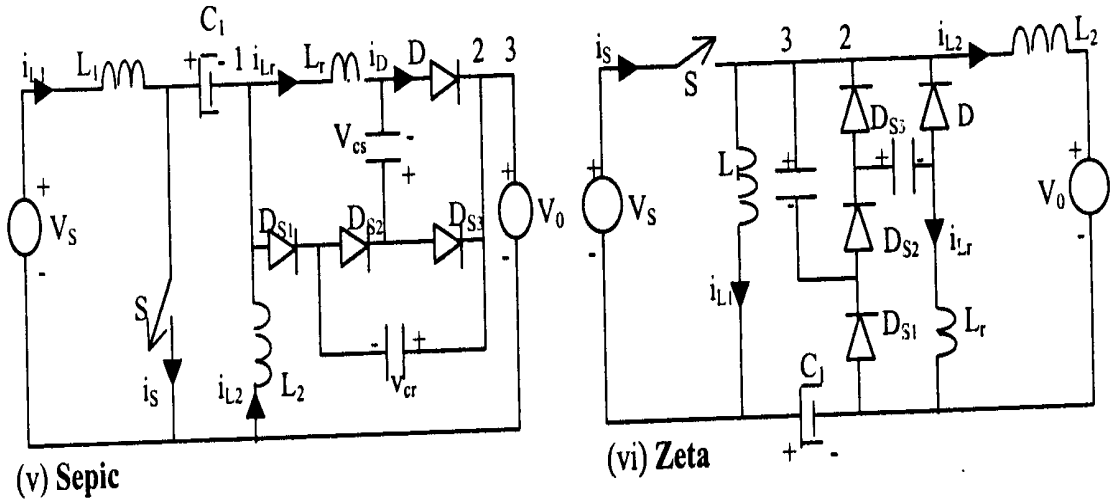


Fig. 2: The Lossless Soft Switched PWM Converters (buck, boost, buck/boost, Cuk's, Sepic and Zeta)

During the on time of the converter active switch S, the free-wheeling diode D is off and during the off time of the active switch S, the diode D is on. The on time and the off time of the active switch S are respectively preceded by the turn on and turn off transients during which current flows for a relatively very short time in the circuit cell. During the on time of the active switch S, the voltage V_{cr} of the resonant capacitor C_r is clamped to the voltage V_{31s} for type A cell and the negative of V_{31s} for type B cell and this clamping ensures that, at the appropriate time, the switch S is turned off at zero voltage. V_{31s} is the voltage between terminals 3 and 1 when S is on. During the subsequent switch turn off transient, the resonant capacitor voltage rises at such a predetermined rate as to eliminate the need for the conventional lossy snubber circuit across the active switch. Also during the turn off transient, the energy stored in the snubber capacitor C_s is returned to the load to allow the turn on of the free-wheeling diode at zero voltage at the end of the turn off transient at which instant V_{cr} becomes clamped (by D_{sl} and D_{s2} conducting) to the voltage between terminals 3 and 2 (V_{32} for type A cell and the negative of V_{32} for type B cell) of the circuit cell. During the off time of the active switch S, therefore, V_{cs} is zero and V_{cr} is V_{32} and the negative of V_{32} for types A and B cells respectively. When S is turned on, the subsequent turn on transient returns (at a rate determined by the value of L_r) the energy in the resonant inductor to the stiff dc voltage V_{21s} (or -V_{21S}) which is the voltage between terminals 1 and 2 of the circuit cell when S is on. The free-wheeling diode is therefore turned off at zero voltage and zero current while the active switch S is turned on at zero current. The rate of fall of the free -wheeling diode current (or the rate of rise of the active switch current) is made low enough by the choice of L_r) as to cause the power loss due to the diode recovery action to be negligible. For the rest of the turn on transient interval, C_r and C_s are made to acquire on time voltages that ensure zero voltage turn off of S and the recovery of the commutation energy at the next turn off transient interval.

3. GENERALISED ANALYSIS OF THE PASSIVELY SOFT - SWITCHED PWM CONVERTER.

In the generalised analysis, the operation of the converter with the type A circuit cell is considered. With the type B circuit cell, the equations derived in the analysis are fundamentally the same. In the analysis, the following assumptions are made:

i. The semi-conductor switches and the passive components are ideal.

ii. The duration of the active switch turn on and turn off transients is so small that during these transients, the converter filter inductor currents remain constant at their values when the turn on

and turn off transients are initiated.

iii. The converter input and output voltages and other filter capacitor voltages are ripple free.

The operation of the soft switched PWM converters is made up of 9 stages in a switching cycle and these 9 stages can be divided into 4 major sections namely:

3.1 The off time of the converter active switch (stage 1), $t_o < t < t_l$:

The off time of the converter active switch is selected here as the first stage of the switching cycle. In this interval, $t_o < t < t_1$ the inductor filter current or the sum of the inductor filter currents flows through a series combination of the resonant inductor L_r and the free wheeling diode D. This current or current sum falls from 12 at $t = t_0$ to I_1 at $t = t_l$ according to the relation.

$t_1 - t_0 = (I_2 - I_1)/K$ (1)

where K is a constant of the converter type During this interval, the resonant capacitor voltage V_{cr} is clamped at V_{32} while the snubber capacitor voltage V_{cs} is zero.

3.2 The active switch turn on transient interval

This is made up of three stages namely:

Stage 2: $t_l < t < t_2$: The converter active switch S is turned on at $t = t_l$ and this places a voltage V_{21s} (positive with respect to terminal 2 of the circuit cell) across L_r in series with D so as to turn off the free wheeling diode at zero current and zero voltage at $t = t_2$.

$t_2 - t_1 = L_r I_1/V_{21s}$ (2)

At the end of this stage, the switch current becomes I_1.

Stage 3: $t_2 < t < t_3$: At $t = t_2$, a resonant current starts to flow in the loop comprising C_r, D_{s2}, L_r, terminal 1 and terminal 3 of the circuit cell. During this resonant mode, the resonant inductor current i_{lr} and the capacitor voltages V_{cr} and V_{cs} are given by the following expressions.

$i_{1r} = (V_{32} - V_{31s})/Z_0 \sin\omega_0(t - t_2)$ (3)

$v_{cr} = (K_s + K_r \cos\omega_0(t - t_2) V_{32}$

$+ K_r V_{31s} (1 - \cos\omega_0(t - t_2))$ (4)

$v_{cs} = -K_s(V_{32} - V_{31s})[1 - \cos\omega_0(t - t_2)]$ (5)

where

$K_s = \omega_{0s}^2/\omega_0^2$, $K_r = \omega_{0r}^2/\omega_0^2$ (6)

$\omega_0^2 = 1/(L_rC_r) + 1/(L_rC_s) = \omega_{0r}^2 + \omega_{0s}^2$ (7)

This stage ends when diode D_{sl} becomes forward biased at $t = t_3$ and starts conducting current thus clamping V_{cr} to V_{31s}.

$v_{cr}(t_3) = V_{31s}$ (8)

The duration of stage 3 can iteratively be determined from equation 8.

Stage 4: $t_3 \le t \le t_4$: During this stage, diodes D_{sl} and D_{s2} are conducting and the resonant inductor current oscillates in the loop comprising D_{sI}, D_{s2}, C_s and L_r until the resonant inductor current becomes zero at $t = t_4$. The resonant inductor current capacitor voltages and the duration of this stage can be shown to be given by the following:

$i_{Ir} = V_s(t_3)/Z_{0s} sin\omega_0(t - t_3) +$
$i_{1r}V_s(t_3)/Z_{0s} cos\omega_0(t - t_3)$ (9)

$v_{cr} = V_{31s}$ (10)

$v_{cs} = v_{cs}(t_3) cos\omega_0(t - t_3) -$
$Z_{0s}\, sin\, \omega_0(t - t_3)$ (11)

$i_{Ir}(t_4) = 0$ (12)

Where:

$\omega_{os} = \frac{1}{L_rC_s}, Z_{os} = \sqrt{L_rC_r}$ (13)

3.3 The active switch on time

(Stage 5): $t_4 \le t \le t_5$: In this interval, the active switch S is carrying the filter inductor current (or the sum of the filter inductor currents). The switch current rises from I_1 at $t = t_4$ to I_2 at $t = t_5$.

$t_5 - t_4 = (I_2 - I_1)/K$ (14)

where K is as defined in equation 1.

3.4 The active switch turn off transient interval: $t_5 \le t \le t_9$

The transient associated *with* the turn off of the active switch S has four stages described as follows:

Stage 6: $t_5 \le t \le t_6$: The switch S is opened at $t = t_5$ and the entire switch current I_2 is diverted to charge the resonant capacitor C_r through diode D_{s1} This charging action makes the switch voltage to rise from zero (at $t = t_5$) at a rate that ensures zero voltage turn off of the switch. The resonant

capacitor voltage during this sub- interval is given by the expression:

$$v_{cr} = I_2(t - t_s)/C_r + V_{31s} \quad (15)$$

Stage 6 ends when diode D_{s3} (with D_{sl} already conducting) becomes forward biased and starts to conduct at t = t_6 and this happens when v_{cr} reaches the voltage value given by

$$v_{cr} = v_{cs}(t_4)C_r + V_{32} \quad (16)$$

The stage 6 interval can therefore be calculated from the relation

$$t_6 - t_5 = [V_{31s} - V_{32} - V_{cs}(t_4)]C_r/I_2 \quad (17)$$

Stage 7: $t_6 \leq t \leq t_7$: In this sub-interval, the current I_2 flowing in and out of the cell circuit splits into two parallel paths consisting of a series combination of D_{sl} and C_r on one hand and the series combination L_r C_r , D_{s3} and V_o on the other hand. During this stage, i_{1r}, v_{cr} and v_{cs} can be shown to be given by

$$i_{1r} = K_r I_2)(1 - cos\omega_0(t - t_6) \quad (18)$$

$$v_{cr} = V_{32} + V_{cr}(t_4) - K_s I_2/(2C_r)\ (t - t_6)$$

$$-K_r Z_{0Is} I_2 sin\omega_0(t - t_6) \quad (20)$$

Where:

$$Z_{0Is} = \sqrt{[L_r C_r/(C_s(C_s + C_r))]} \quad (21)$$

Stage 7 ends at t = t_7 when D_{s2} becomes forward biased so that the conduction of all the three snubber diodes clamps V_{cr} to V_{32}.Therefore, the sub-interval (t_7 – t_6) can be determined form the relation.

$$v_{cr}(t_7) = V_{32} \quad (22)$$

Stage 8: $t_7 \leq t \leq t_8$: In this stage, all the snubber diodes conduct and the resonant inductor current rises from its value at t = t_7 to I_2 at t = t_8. i_{1r} and V_{cs} in this interval are given as:

$$i_{Ir} = i_{Ir}(t_7)cos\omega_{os}(t - t_7) + v_{cs}(t_7)Z_{os}sin\omega_{os}(t - t_7) \quad (23)$$

$$v_{cs} = v_{cs}(t_7)cos\omega_{os}(t - t_7) - i_{Ir}(t_7)Z_{os}sin\omega_{os}(t - t_7) \quad (24)$$

The duration of stage 8 in seconds can be obtained from the relation.

$$i_{Ir}(t_8) = I_2 \quad (25)$$

Stage 9: $t_8 \leq t \leq t_9$: In this stage, all snubber diodes stop conducting and the current I_2 charges the capacitor C_r and this charging continues until V_{cs} is decreased from its value at t = t_8 to zero at t = t_9

$$t_9 - t_8 = C_s v_{cs}(t_8)/I_2 \quad (26)$$

At t = t_9, the free wheeling diode D becomes forward biased and the current I_2 is instantaneously transferred to it at zero voltage.

Time Variation of Selected Circuit Currents and Voltages:

The time variation of i_{1r} , V_{cr} , V_{cs}, the free wheeling diode current i_D and the switch current i_s are shown in Fig. 3 for converters with type A circuit cells while Table 1 shows the relevant circuit voltages and currents for the various converter topologies in Fig. 2.

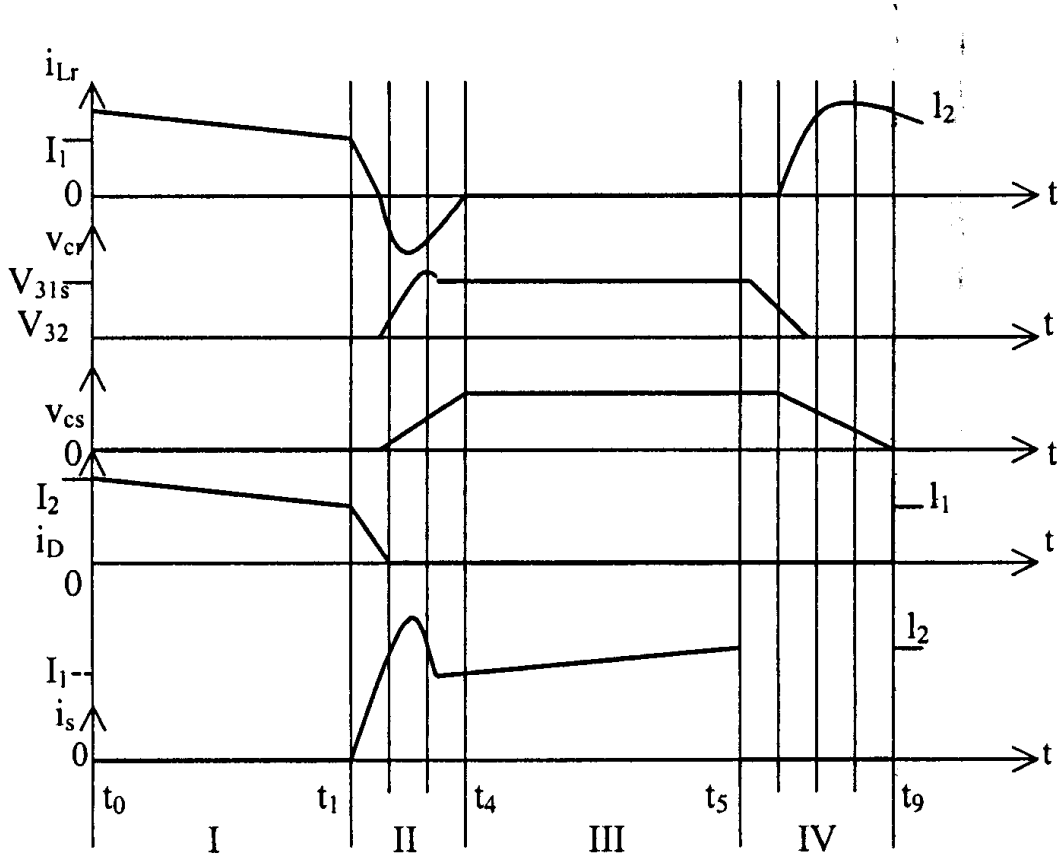


Fig. 3: i_{Lr}, v_{cr}, v_{cs}, i_D and i_s for converters using Type A Cell

Adaptation of Analysis to Type B Circuit Cell:

Equations 1 to 26 become the circuit equations of type B circuit cell in the basic converter types if V_{21s}, V_{31s}, and V_{32} in these equations are replaced by their negative values ($-V_{21s} > -V_{31s}$ and $-V_{32}$) respectively. Also, the time variation of i_{1r} , V_{cr}, v_{es}, the free wheeling diode current i_D and the switch current is for converters with type B circuit cell only differs from that of converters with type A cell in the V_{cr} waveform because with type B cell, V_{cr} falls from $-V_{32}$ to $-V_{31s}$ during the turn on transient and does the reverse during the turn off transient

CONCLUSION

A unified analysis approach for designing and predicting the performance of the basic converter passively soft-switched by a versatile circuit cell has been presented in this paper. The unified analysis has been shown to be applicable to twelve converter topologies created using the circuit cell. Neglecting the very short duration of the active switch transient current during its turn on transient, the converter active switch and free wheeling diode current and voltage stresses remain the same as those of the hard-switched converter. With this minimum current and voltage stresses, relatively simple control circuit and near loss less switching features, the converter discussed has the potential of wide industrial applications.

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Table 1: Circuit Voltages and Currents for the Converter Topologies in Fig. 2

Converter Type	Current I_1 [$I_1 = i_D(t_l)$]	Current I_2 [$I_2 = i_s(t_5)$]	V_{21s} (V_{21}, $t_l \le t \le t_5$	V_{31s} (V_{31},tl $\le t \le t_5$	V32	Cell Type
Buck						
a	$i_L(t_1)$	$i_L(t_5)$	$-v_s$	$-V_s$	0	B
b	"	"	$-V_s$	0	V_s	B
c	"	"	$-v_s$	V_o-V_s	V_o	B
Boost						
a	$i_L(t_l)$	$i_L(t_5)$	Vo	0	-Vo	A
b	"	"	Vo	Vs	$v_s v_s$	A
c	"	"	Vo	Vo	0	A
Buck/Boost						
a	$i_L(t_l)$	$i_L(t_5)$	-Vo	- Vs	V_0	B
b	"	"	$-(V_S+V_O)$	0	V_s-V_s	B
c	"	"	$-(V_s+V_O)$	$-(V_s+V_o)$	0	B
Cuk's	$i_{L1}(t_l) + i_{L2}(t_l)$	$i_{Ll}(t_5) + i_{L2}(t_5)$	$-v_s$	0	V_{cl}	B
Sepic	$i_{L1}(t_l) + i_{L2}(t_l)$	$i_{L1}(t_l) + i_{L2}(t_l)$	$V_{cl}+V_0$	$V_{cl} +V_o$	0	A
Zeta	$i_{L1}(t_l) + i_{L2}(t_l)$	$i_{L1}(t_l) + i_{L2}(t_l)$	V_{cl}	V_{cl}	0	A