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FUNDAMENTALS OF A MULTI-PHASE, NEUTRAL-POINT CLAMPED MULTILEVEL INVERTER

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ABSTRACT
The conventional five-level diode-clamped inverter suffers from the problem of many active power switches when extended to multiphase system. As a consequence, increasing number of gate drive circuits are required; resulting in complex system circuitry. This paper presents the fundamentals of a multiphase, neutral point clamped multilevel inverter configuration capable of reducing the number of active power switches in the conventional topology for multiphase system. The proposed multilevel inverter configuration generates five line-to-line voltage levels for multiphase systems. From the generalized model, an exemplary 5-phase, 5-level line-line NPC inverter supplying an RL load is considered. The operational and modulation principles and the switching patterns are outlined. The THD, as a performance index, of the line voltage output waveform of the proposed 5-phase, 5-level line-line NPC inverter is similar to that of the corresponding well-known conventional 5-phase, NPC diode-clamped inverter. The proposed inverter achieves this with fewer power circuit components and simplicity. The validity of the proposed multilevel inverter is verified through simulations and experimental results.

Keywords: *inverter, multilevel, harmonics, total harmonic distortion, multi-phase.*

1. INTRODUCTION
Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, et cetra, can be easily interfaced to a multilevel converter system for a high power application [1-3].

The concept of multilevel converters has been introduced since 1975 [4]. The term multilevel began with the three-level converter [5]. Subsequently, several multilevel converter topologies have been developed [6-13]. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel converter can be briefly summarized as follows.

1. Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced.
2. Common-mode (CM) voltage: Multilevel converters produce smaller CM voltage;

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therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies such as that proposed in [14].

3. Input current: Multilevel converters can draw input current with low distortion.
4. Switching frequency: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

Many multilevel converter applications focus on industrial medium-voltage motor drives [3, 11, 15], utility interface for renewable energy systems [16], flexible AC transmission system (FACTS) [17], and traction drive systems [18]. Unfortunately, multilevel converters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a multilevel converter, each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex.

In electrical drive applications, three-phase drives are widely used for their convenience. However, multiphase drives possess several advantages over conventional three-phase drives such as: reducing the amplitude and increasing the frequency of torque pulsations, reducing the rotor harmonic currents, reducing the current per phase without increasing the voltage per phase, and lowering the dc-link current harmonics and higher reliability. By increasing the number of phases, it is also possible to increase the torque per rms ampere for the same volume machine [19].

Applications involving high power may require multiphase systems, in order to reduce stress on the switching devices. There are two approaches to supplying high power systems; one approach is the use of multilevel inverters supplying three-phase machines and the other approach is multi-leg inverters supplying multiphase machines. Much more work has been done on multilevel inverters. It is interesting to note the similarity in switching schemes between the two approaches: for the multilevel inverter the additional switching devices increase the number of voltage levels, while for the multiphase inverter, the additional number of switching devices increases the number of phases [20]. Power rating of the inverter should meet the required level for the machine and driven load. However, the inverter ratings cannot be increased over a certain range due to the limitation on the power rating of semiconductor devices. One solution to this problem is using multi-level inverter where switches of reduced rating are employed to develop high power level converters. The advent of inverter fed motor drives also removed the limits of the number of motor phases. This fact made it possible to design machine with more than three phases and brought about the increasing investigation and applications of multi-phase motor drives [21, 22].

Modulation control of multiphase multilevel inverters is quite challenging, and much of the reported research is based on somewhat heuristic investigations [23, 24]. By and large, the emphasis has been placed on space vector PWM (SVPWM) methods. SVPWM offers great flexibility to optimize switching waveforms and is suited for digital implementation.

The diode-clamped inverter topologies, published by different researchers [25, 26] in the early 90's can be deemed as the extension of the neutral-point-clamped (NPC) inverter introduced in the early 80's [5]. The principle of improving the quality of the waveform of the classical inverter by inserting an auxiliary circuit between the source and the power switches of the basic full-bridge inverter has been reported in the literature for single-phase inverters, in [27–31]. Based on this principle, a modified NPC three-phase, three-level inverter configuration was proposed in [32]; wherein the THD of the inverter output voltage waveform was drastically reduced through analyses at fundamental frequency switching and reduced power circuit component count.

Recently, conventional three-level (NPC) five-phase inverters are employed for five-phase single motor drive [33] and five-phase two-motor drives [34]. Large numbers of space vectors are generated due to highly complex power circuit topology of three-level inverters. The developed PWM schemes for three-level, five-phase inverters pose real time implementation challenges due to limited capability of the signal processors.

Thus, this paper presents the fundamentals of a generalized multiphase, NPC multilevel inverter topology which reduces the number of active power circuit switches and complexity in conventional NPC multiphase inverters. For the purpose of amplitude and frequency variation of the output voltage, the carrier-based sinusoidal pulse width modulation

(SPWM) is employed in the generation of the proposed inverter gating signals.

From the generalized configuration, an exemplary circuit of 5-phase, NPC inverter supplying an RL load is presented. The proposed inverter operational principles and modulation scheme are given. Simulation and experimental results are adequately presented to verify the validity of the proposed 5-phase, 5-level line-line, SPWM inverter configuration.

2. CIRCUIT CONFIGURATION OF THE PROPOSED MULTIPHASE NPC INVERTER.

The generalized power circuit configuration of the proposed multiphase NPC inverter is shown in Figure 1(a). It is a modification of the basic 2-level inverter configuration; where an auxiliary circuit is inserted per phase leg. Each auxiliary circuit constitutes one switching element and full-bridge diodes. The dc source is split into two equal parts by capacitor banks; hence forming the neutral point, n. For each phase, one terminal of the auxiliary circuit is connected to the neutral point, n; while the other terminal of the auxiliary circuit is hooked to the centre of the respective phase-leg. In all, only three active switches are utilized per phase leg.

For the first phase leg in Figure 1(a) and (b), the synthesized voltage levels, with respect to the neutral point, and the corresponding switching states of the active power semiconductor switches in both conventional and the proposed multiphase inverters are summarised in Table 1.

Shown in Figure 1 (b) is the well known multiphase NPC inverter topology. It is obvious that two active switches are needed to clamp the respective phase voltage to the neutral point, n.

Obviously in Figure 1(a), the number of inverter leg, with the corresponding auxiliary circuit, equals the number of phases,

N, in the system. Each phase is displaced by an angle θ from its preceding phase.

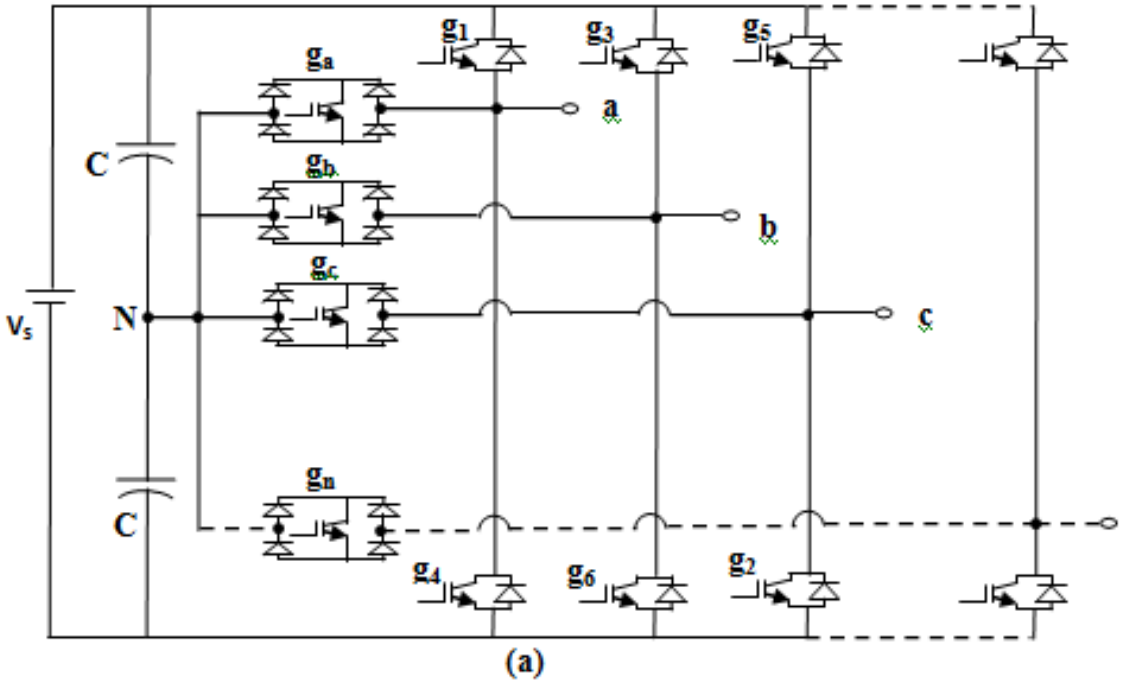
$$\theta = \frac{2\pi}{N} \qquad (1)$$

Table 1(a): Definition of switching states for the proposed NPC multiphase inverter.

Phase voltage, V_{an}	Switching states		
	g_1	g_a	g_4
$\frac{V_s}{2}$	on	off	off
0	off	on	off
$-\frac{V_s}{2}$	off	off	on

Table 1(b): Definition of switching states for the conventional NPC multiphase inverter.

Phase voltage, V_{an}	Switching states			
	g_{1a}	g_{2a}	$\overline{g_{1a}}$	$\overline{g_{2a}}$
$\frac{V_s}{2}$	on	on	off	off
0	off	on	on	off
$-\frac{V_s}{2}$	off	off	on	on



(a)

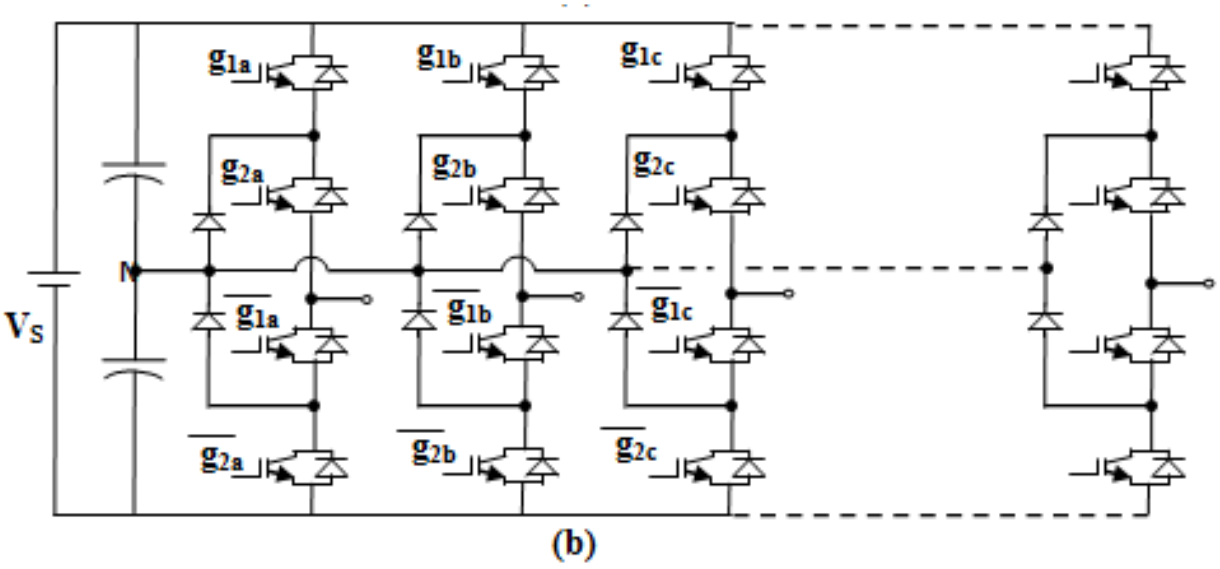


Figure 1: Configuration of the proposed and conventional NPC multiphase voltage source inverter: Proposed NPC multiphase inverter. (b) Conventional NPC multiphase inverter.

3. PWM MODULATION SCHEME

The carrier-based modulation scheme for multilevel inverters is adopted in the generation of the gating pulses for the proposed inverter topology for ease of implementation in an analogue circuit. Precisely, the in-phase disposition (IPD) modulation technique of the level-shifted multicarrier modulation scheme is used, since it provides the best harmonic profile of all the multicarrier modulation schemes, [35, 36]. In this modulation scheme, a multilevel inverter with *m* voltage levels requires (*m*-1) triangular carriers; all having the same frequency, phase and amplitude. The (*m*-1) triangular carriers are vertically disposed such that the bands they occupy are contiguous. For a desired number of phase system, n, the modulating signal is usually an *n*-phase sinusoidal wave with adjustable amplitude and frequency. In the context of this paper, *m* is 3. The gate signals are generated by comparing the modulating wave with the carrier waves. The frequency modulation index is given by

$$m_f = \frac{f_c}{f_m} \tag{2}$$

Where f_c and f_m are the frequency of the carriers and the modulating signals, respectively.

Whereas the amplitude modulation index is defined as

$$m_a = \frac{V_m}{V_c(m-1)} \tag{3}$$

Where V_m and V_c are the peak amplitude of the modulating wave and peak amplitude of each carrier wave.

In order to typify the aforementioned generalized approach, a 5-phase, 5-level line-line inverter system is considered in which case $N = \mathrm{n} = 5$, $m = 3$ and $\theta = 72^\circ$. In effect, five sinusoidal modulating signals, with phase difference of 72°, have to be compared with two triangular carrier waves placed above and below the zero point in the x-y plane.

Figure 2 shows the switching scheme that generated the six gating pulses: g_1, g_a, g_4, g_3, g_b and g_6, for phase 'a' and 'b' power switches. Therein also, the synthesized phase voltages, v_{an} and v_{bn} are shown. The resulting line voltage, v_{ab} is clearly the difference of the two phase voltage waveforms. Gating pulses and phase voltages for phase c, d, and e are obtained by similar comparison of v_{mc}, v_{md} and v_{me} with the triangular carrier signals. With these, all the line voltages will be synthesized.

The logical expressions from which the gating pulses of phase A: g_1, g_a and g_4, are derived are given in equations (4) through (6).

$$g_1 = v_{ma} > T_U \tag{4}$$

$$g_a = \left\{ \begin{matrix} \left[(v_{ma} < T_U)\ AND\ (v_{ma} > 0) \right] \\ OR\ \left[(v_{ma} > T_L)\ AND\ (v_{ma} < 0) \right] \end{matrix} \right\} \tag{5}$$

$$g_4 = v_{ma} < T_L \tag{6}$$

Analytical expressions for the average conduction power losses in the main power semiconductor switches can be obtained in terms of the voltage and current amplitudes, depth of modulation and power factor for typical conditions prevailing in pulse width modulated inverters, [37]. For each of the active

switches (IGBT) used herein, a good approximation for the average on-state loss, P_S, is

$$P_S = \frac{V_{TO} I_m}{2\pi}\left\{1+\frac{\pi}{4} M_a \cos\phi\right\} \quad (7)$$

where $V_{TO}, I_m, M_a \text{ and } \phi$ mean the constant on-state voltage across a switch, peak load current through a device, applied modulation index and power factor angle, respectively.

Also, the conduction loss, P_D, for the diodes across the auxiliary switches, per phase, subjected to constant on-state voltage of $\frac{V_S}{2}$ can be given as

$$P_D = \frac{V_S I_m}{\pi}\left\{1-\frac{\pi}{4} M_a \cos\phi\right\} \quad (8)$$

Equations (7) and (8) can be normalized to have the contour plots of $\frac{2\pi}{V_{TO} I_m} P_S$ and $\frac{\pi}{V_S I_m} P_D$ against the modulation index and the load power factor as depicted in figure (3). The switch losses can be seen in figure 3 (a) increasing while the diode losses in figure 3 (b) decreases complimentarily as the load power factor improves. Similar trends are apparent as depth of modulation increases.

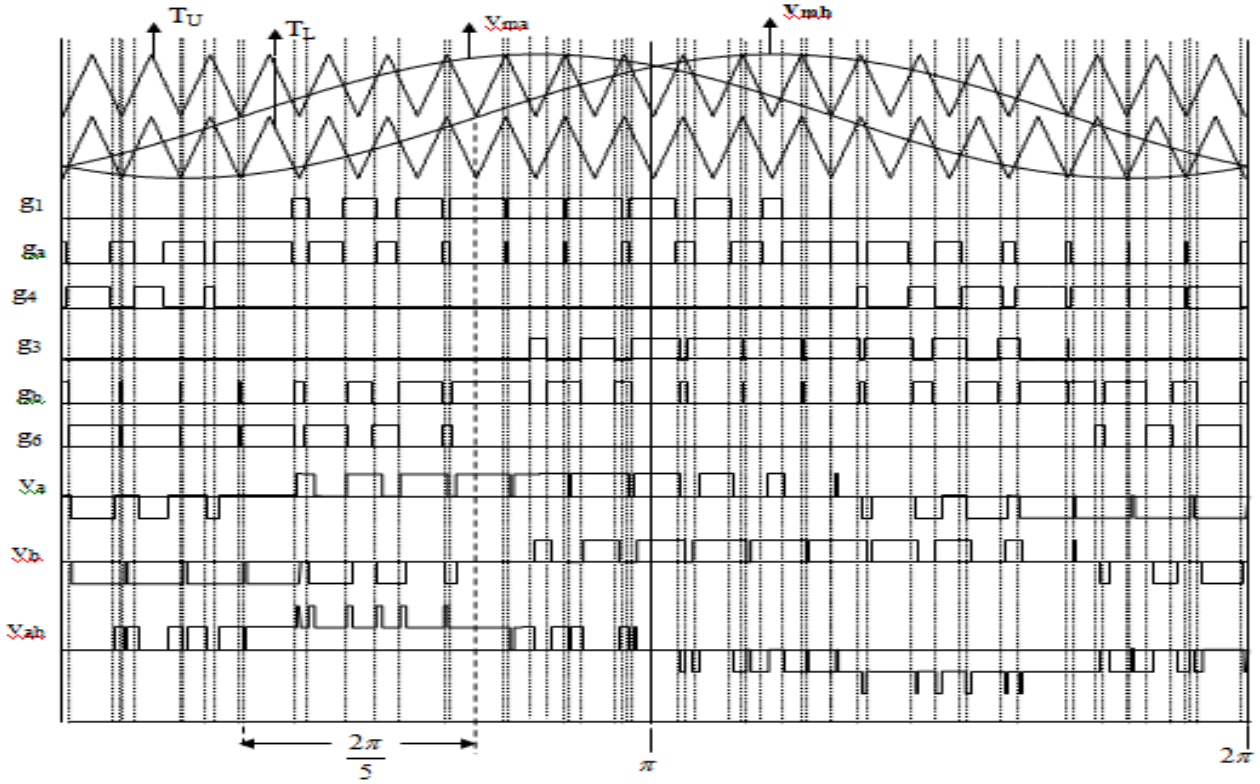
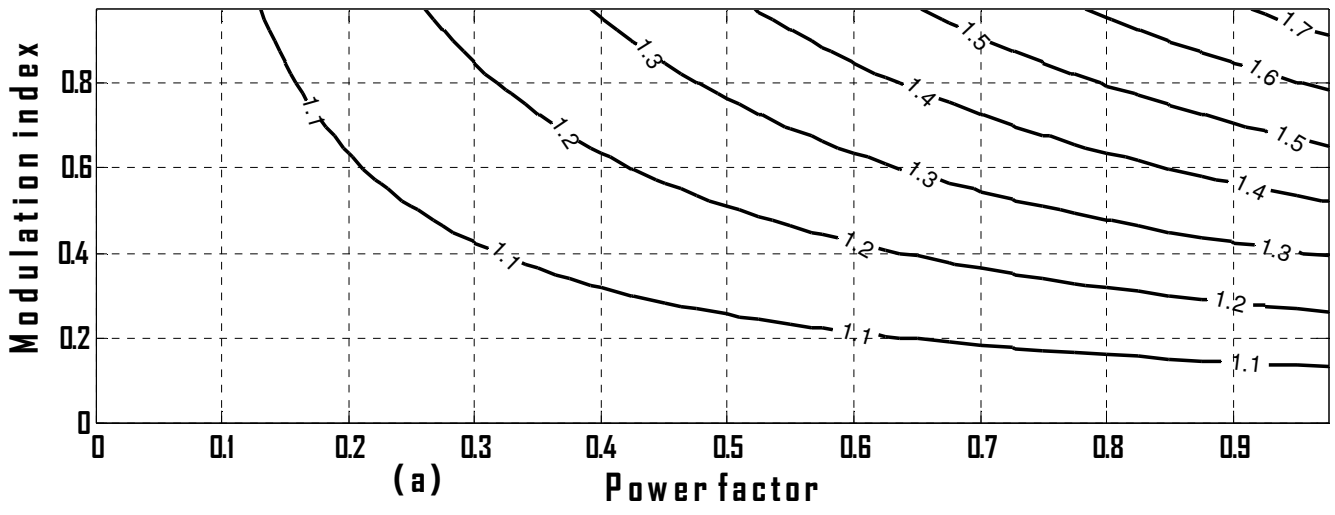


Figure 2: Switching patters and output voltages of the proposed multi-phase, NPC PWM inverter



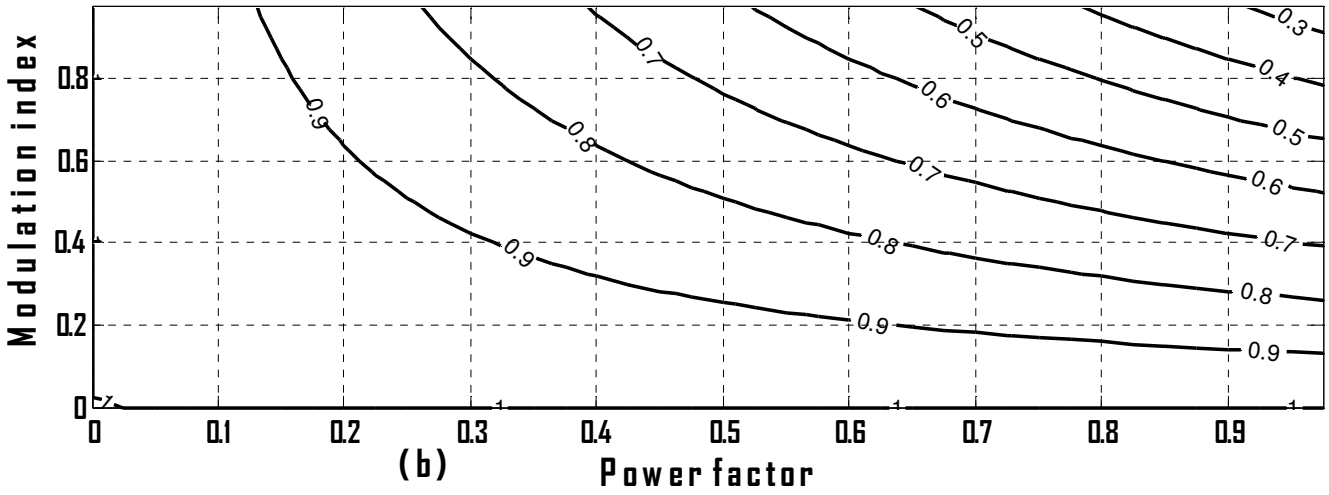


Figure. 3: Normalize values of conduction losses, P_S and P_D, and their variation with power factor and depth of modulation. (a) P_S. (b) P_D.

4. SIMULATION AND EXPERIMENTAL RESULTS

4.1. Simulation results

From the generalized circuit model in Figure 1(a), MATLAB SIMULINK simulated the proposed exemplary 5-phase NPC inverter topology in accordance to the carrier-based PWM switching scheme presented in Figure 2. A balanced five-phase star connected RL load with 10Ω resistance and 96mH inductance per phase were used for an input voltage of 400V.

Figures 4 and 5 show the simulated inverter output phase and line voltage waveforms at carrier frequency of 1kHz and modulation index of 0.85.

The phase voltage waveforms exhibit three levels: $\frac{V_S}{2}, 0, \frac{-V_S}{2}$; while the line-to-line voltage waveforms show five levels: $V_S, \frac{V_S}{2}, 0, \frac{-V_S}{2}, -V_S$ as earlier predicted. For the indicated loading condition, the simulated output line current waveforms are shown in Figure 6.

The performance index namely total harmonic distortion (THD) is chosen to assess the quality of the synthesized inverter output waveforms. Spectral analysis of the inverter line voltage waveform in Figure 4 is carried out. The spectral results are displayed in Figure 7; wherein a total harmonic distortion (THD) value of 46.62% is achieved in the line voltage waveform.

Under the same simulation conditions and voltage level, the generalized conventional NPC multiphase inverter topology, shown in Figure 1(b), is configured for five phase system and simulated. The spectral analyses results of the synthesized line voltages are shown in Figure 8. This is in accordance with the results in [36] for classical NPC inverter; though for three phase system. Moreover, for the specified loading condition, a THD of 3.71% is obtained in the output line current, i_a; as shown in Figure 9.

With respect to obtaining a quasi sinusoidal voltage waveform at the output terminal, it is now obvious that the proposed NPC inverter topology performance is at par with that of the conventional NPC inverter configuration.

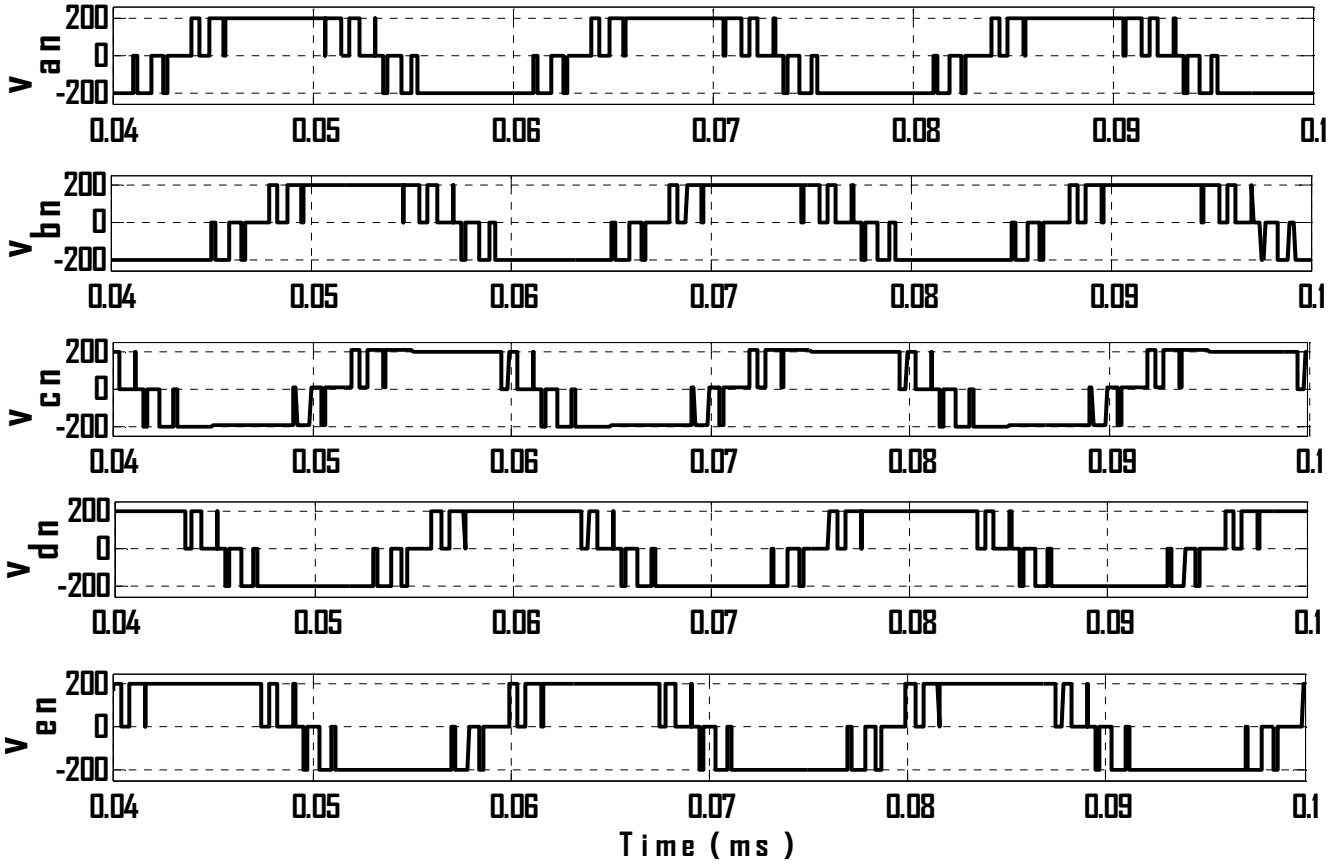


Figure 4: Simulated Inverter Output Phase Voltages.

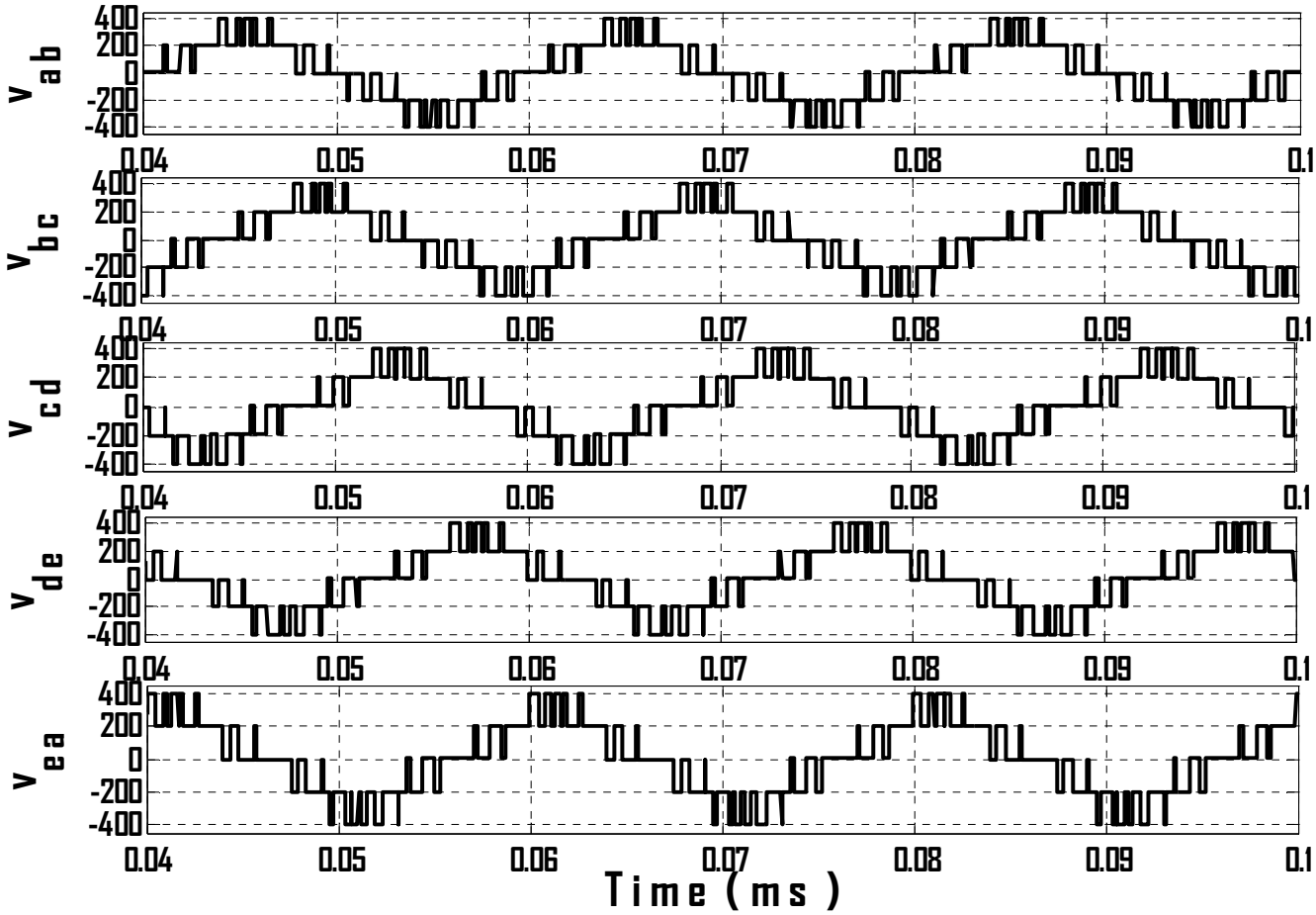


Figure 5: Simulated Inverter Output Line Voltages.

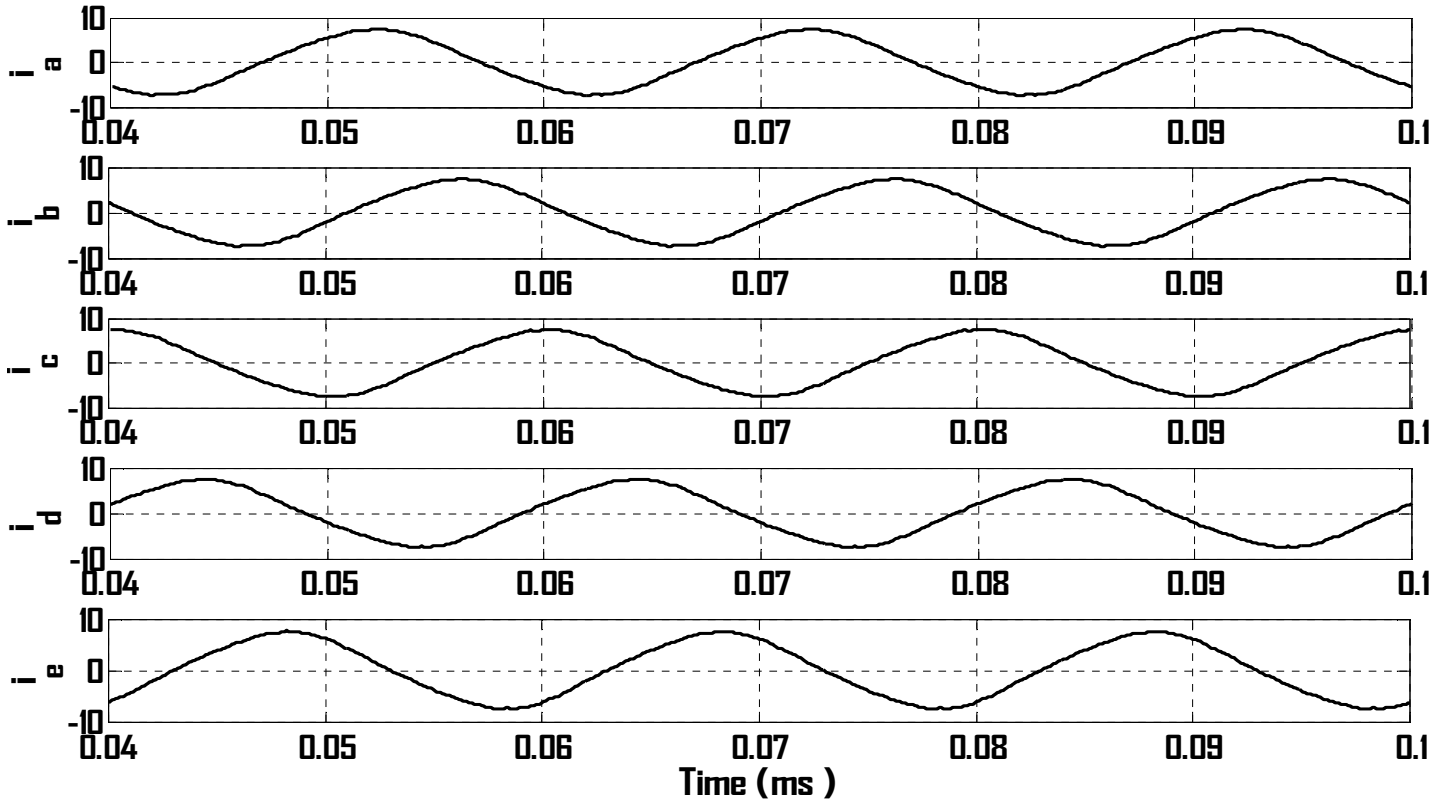


Figure 6: Simulated Inverter Output Line currents.

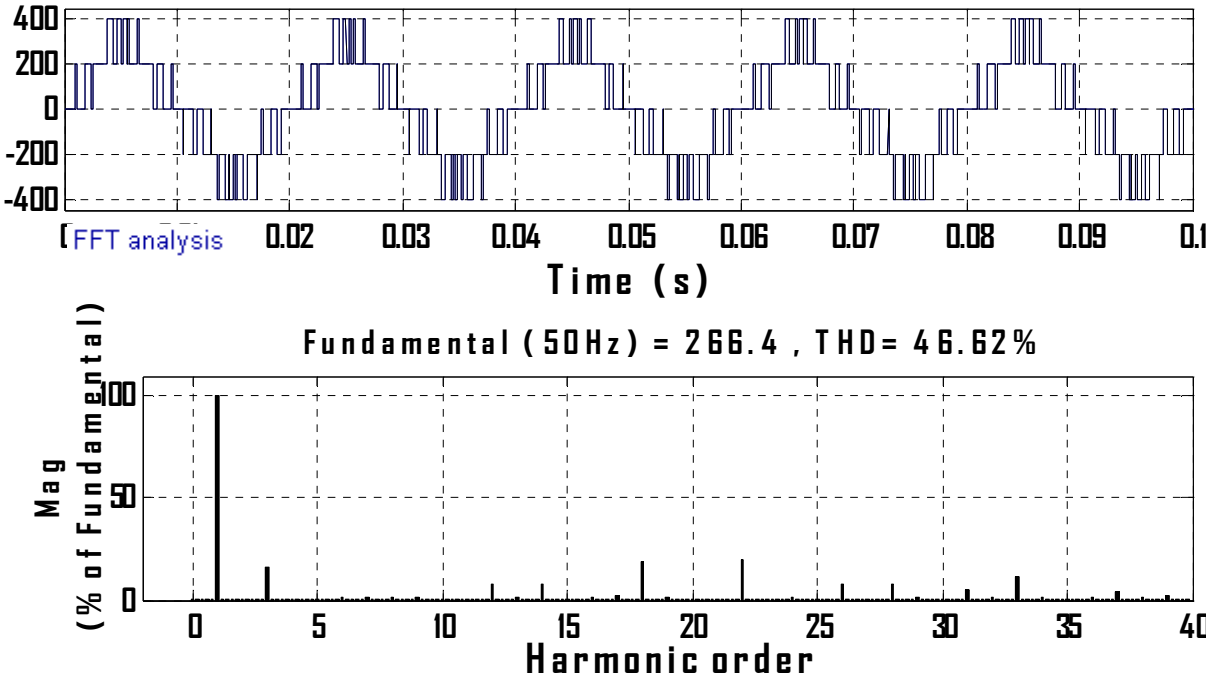


Figure 7: FFT analyses of the synthesized output line voltage of the proposed NPC 5-phase inverter.

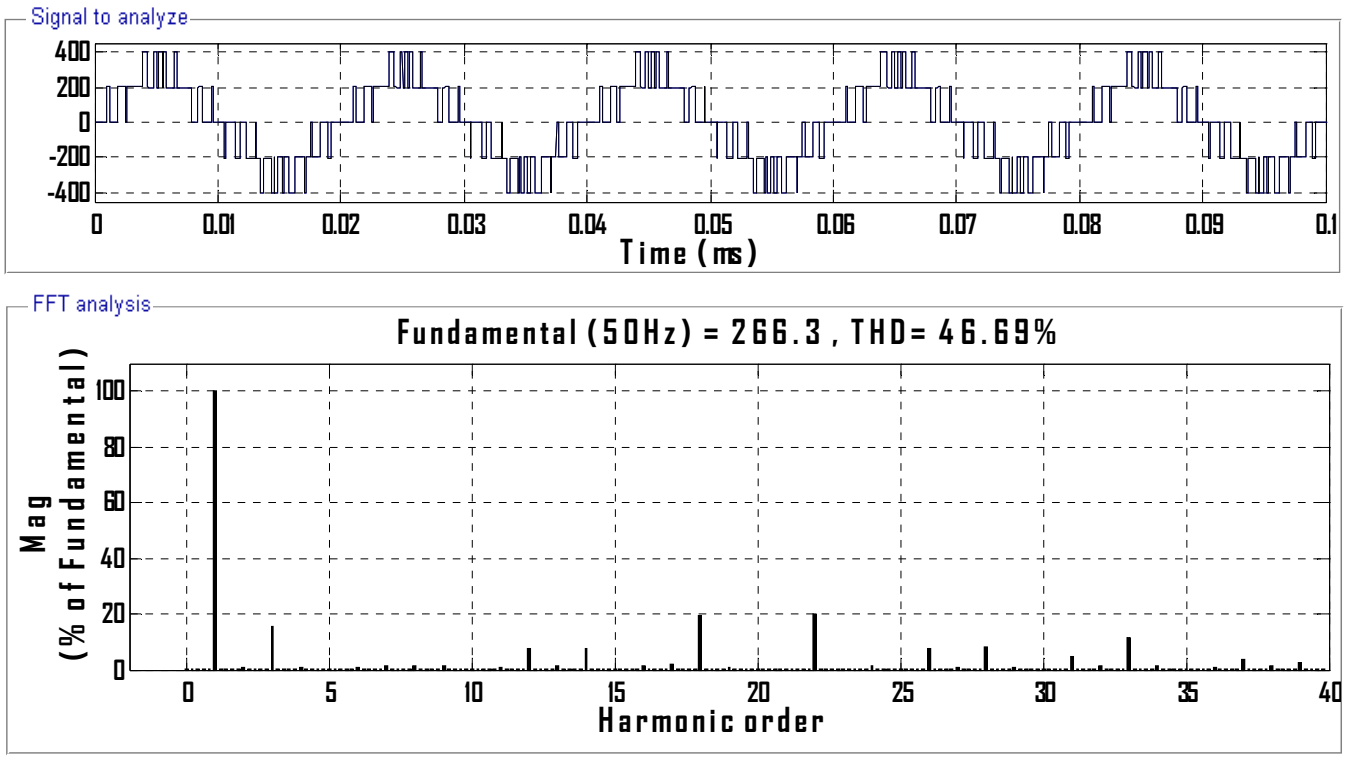


*Figure 8: FFT analyses of the synthesized output line voltage of the conventional NPC 5-phase **inverter***

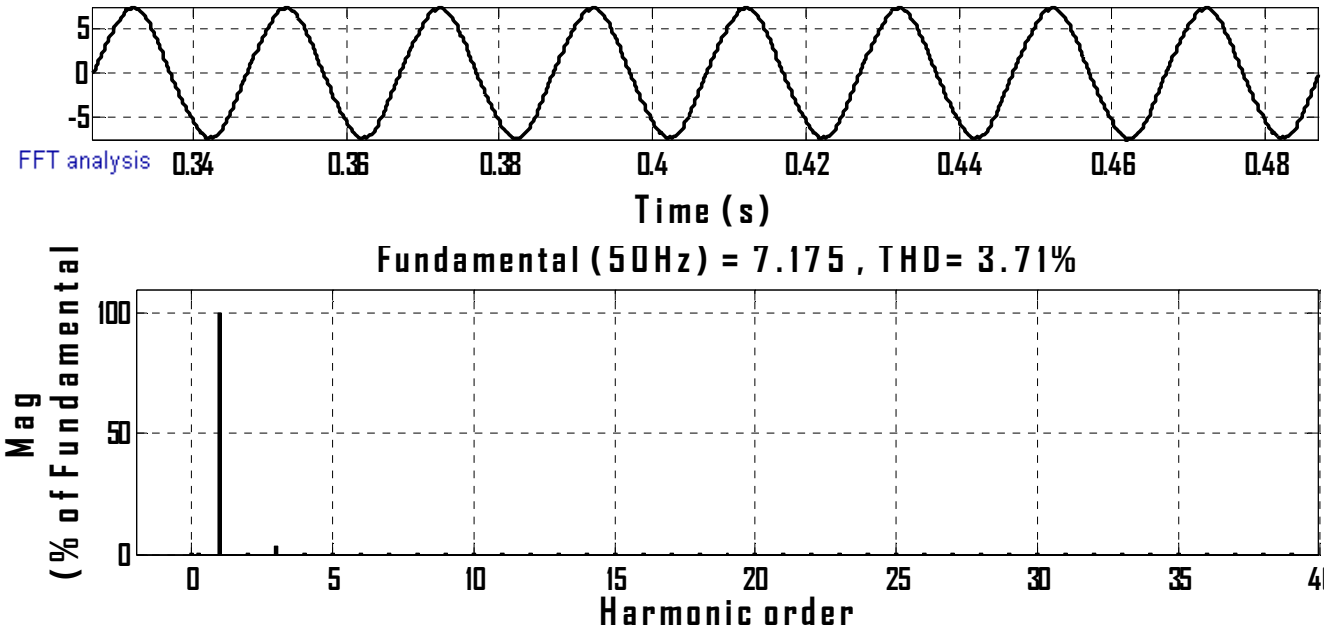


Figure 9: FFT analyses of one of the output line current of the proposed NPC 5-phase inverter.

4.2 Experimental results

A scaled laboratory prototype has been built for verification of the exemplary 5-phase NPC multilevel inverter. A 400 V stiff dc power source is employed as the dc supply for the input voltage. As the load for the inverter, a 96 mH inductor in series with a 10Ω resistor are connected at the output terminal of each phase; the other terminals of the loads are hooked together, forming a star point. The carrier frequency is 1kHz and the modulation index is 0.85. Basic CMOS logic gates and TL 084 IC were deployed in the generation of the inverter 15 gating pulses; of which six were specified in Figure 2 for phase a and b. The laboratory prototype set-up of the proposed three-phase inverter is shown in Figure 10; comprising the logic, driver and power circuits. Most interesting in the proposed inverter configuration is the simplified circuit and ease of implementation.

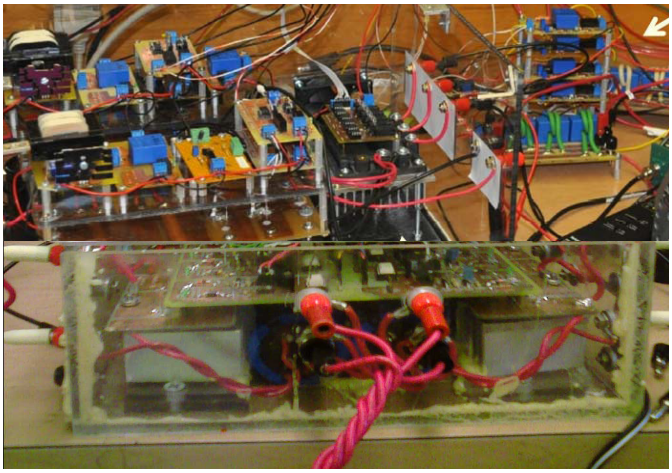


Figure 10: Laboratory prototype setup for the proposed five-phase, five-level multilevel inverter.

Figure 11 shows experimentally obtained gating signals for the switches of one of the inverter legs: g_1, g_a and g_4. The prototype specification is given in Table 2. Shown in Figure 12 are the experimental waveforms of four of the five output phase voltages: v_{an}, v_{bn}, v_{cn}, and v_{dn}. The corresponding experimental waveforms for the line voltages v_{ab}, v_{bc}, v_{cd}, and v_{de} are shown in Figure 13. For a cycle, these voltage waveforms exhibit three and five levels as earlier proposed for the phase and line voltages, respectively. For the loading condition specified in Table 2, the corresponding experimental output line currents are shown in Figure 14. The extent of distortion in the line current waveform is verified and the FFT analysis is shown in Figure 15.

Table 2: Prototype specification.

Power switches: IGBT EUPEC BSM 75 GB 120DLC
Fast switching diodes in the auxiliary circuits:
R = 10Ω , L = 96Mh
C = 5000μF, 600V

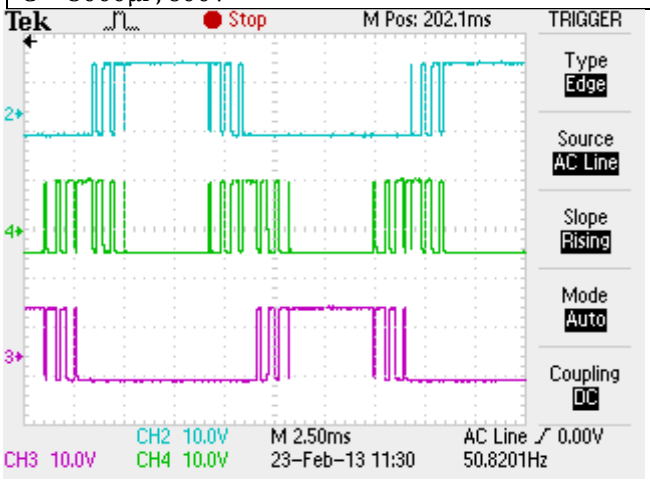


Figure 11: Experimental gate signals for phase A: g_1(channel 2), ga(channel 3), and g_4(channel 3).

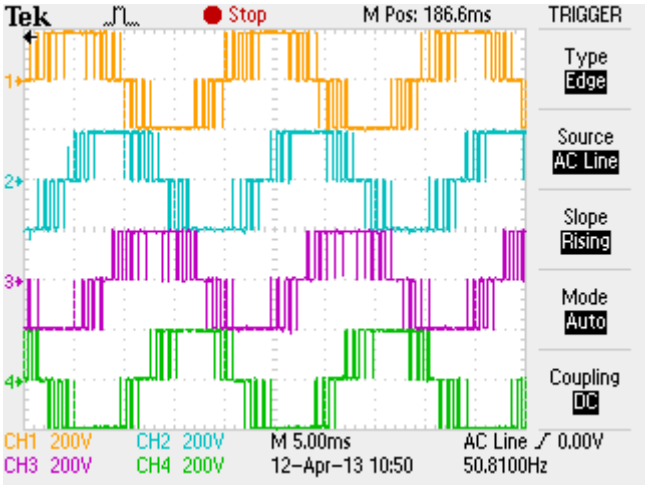


Figure 12: Experimental inverter phase van, vbn, vcn, and vdn output voltages

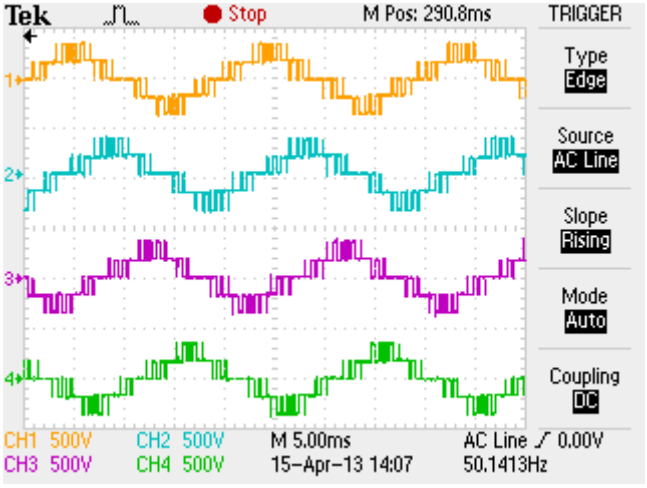


Figure 13: Experimental inverter line v_{ab}, v_{bc} , v_{cd}, and v_{de}, output voltages.

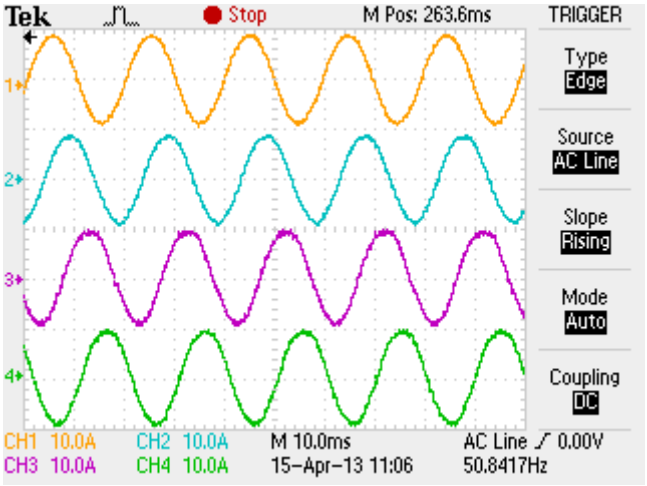


Figure 14: Experimental inverter line i_a, i_b, i_c and i_d currents.

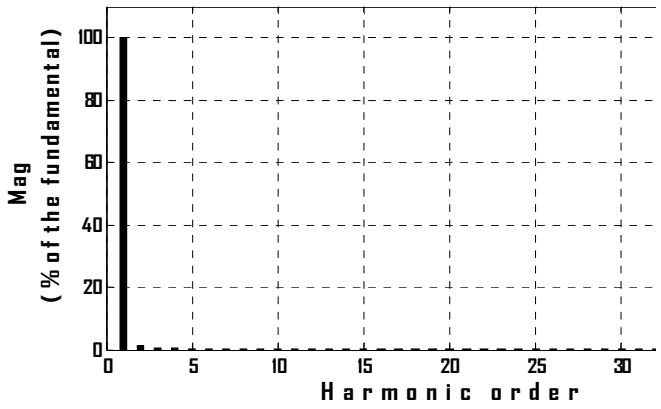


Figure 15: FFT analyses of the experimental output line, i_a, current of the proposed NPC 5-phase inverter.

5. CONCLUSIONS

This paper has presented the fundamentals of a multi-phase, neutral-point clamped multilevel inverter. The proposed generalized configuration accommodates as much system phase as needed for five-level output line voltage waveform at reduced power circuit component count. A 5-phase, 5-level line-line multilevel inverter has been extracted from the generalized model as a demonstrative configuration. The operational principles and switching functions generation have been discussed in detail. Simplified sinusoidal pulse width modulation technique, suitable for analogue circuit implementation, has been employed in the synthesis of the firing gate pulses for the active power switches. The presented 5-phase, 5-level line-line multilevel inverter exhibited similar behaviors of the conventional diode-clamped inverter earlier reported, but with reduced active power switches and ease of implementation. The spectral analyses of the synthesized output line voltages were given. It has been shown that the harmonic spectrum performance of the proposed inverter is quite at par with those of the diode-clamped inverter. However, the proposed inverter topology presents a power circuit of reduced component count.

Simulation and experimental results obtained validated the proposed five-phase, NPC, PWM multilevel inverter topology.

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