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IMPROVEMENT OF POWER SYSTEM QUALITY USING VSC-BASED HVDC TRANSMISSION

O. J. Eyenubo[1,*] and P. Oshevire[2]

[1] DEPT. OF ELECTRICAL/ELECTRONIC ENGINEERING, DELTA STATE UNIVERSITY, OLEH CAMPUS, DELTA STATE NIGERIA
[2] DEPT. OF ELECTRICAL/ELECTRONIC ENGR, FEDERAL PETROLEUM UNIVERSITY, EFFURUN DELTA STATE, NIGERIA.
E-mail addresses: [1]*eyenubo63@yahoo.com,* [2]*ask4pat2001@yahoo.com*

ABSTRACT

The HVDC technology can be represented by the combination of a Direct Current (DC) circuit with two power electronics converters, each one at a link terminal, for AC/DC and DC/AC conversion The principal characteristic of VSC-HVDC transmission is its ability to independently control the reactive and real power flow at each of the AC systems via the Point of Common Coupling (PCC). The active and reactive power is related to the power angle and the magnitude of voltage in the reference $d-q$ ***-frame selected such that the quadrature component will result in the ratio between the maximum fundamental peak phase voltage and the DC total voltage.***

Key words*: HVDC, Voltage source converter (VSC), Current and Voltage Control Loop; FFT Analysis*

Nomenclature

HVDC	High-voltage direct current
HVAC	High voltage alternating current
CSC	Current source converters
VSC	Voltage source converters
PCC	Point of common coupling
FFT	Fast Fourier Transform
GTO	gate turn-off thyristors
α	real part space vector components
β	imaginary part space vector components
$"d"$	direct axis
$"q"$	quadratic axis
i_{vd}, i_{vq}	current components
I_{dq}	converter current vector
Id_0	midpoint current
Ud_0	midpoint voltage

1. INTRODUCTION

A high-voltage direct current (HVDC) electric power transmission system uses direct current for the bulk transmission of electrical power in contrast with the more common alternating current systems. The HVDC technology can be represented by the combination of a DC (Direct Current) circuit with two power electronics converters each one at a link terminal for AC/DC and DC/AC conversion; the DC circuit can consist of a cable, a line or simply a capacitor [1].

This technology has the characteristic that is widely attractive over High Voltage Alternating Current (HVAC) transmission for specific applications, such as long distance power transmission, long submarine cable links and interconnection of asynchronous systems. The speed and flexibility of the HVDC technology is able to provide the transmission system with several advantages such as transfer capacity enhancement, power flow control, transient stability improvement, power oscillation damping, voltage stability and control and rejection of cascading disturbances. Recent advances in power electronics coupled with HVDC traditional features leads to a further deployment of this technology to improve system operation and support the development of onshore and possibly offshore European transmission grids [2, 3].

The main requirement in a power transmission system is the precise control of active and reactive power flow to maintain the system voltage stability. This is achieved through an electronic converter and its ability of converting electrical energy from AC to DC or vice versa. There are basically two configuration types of three-phase converters possible for this conversion process, Current Source Converters (CSC) and Voltage Source Converters (VSC). Modern HVDC transmission systems

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Corresponding author tel: + 234-816-739-3531

can utilize either traditional CSC or VSC as the basic conversion means. The increasing rating and improved performance of self-commutated semiconductor devices have made possible High Voltage DC (HVDC) transmission based on Voltage-Sourced Converter (VSC). Two technologies offered by the manufacturers are the HVDC Light and the HVDC [4].

2. DESCRIPTION OF VSC-BASED HVDC LINK

The principal characteristic of VSC-HVDC transmission is its ability to independently control the reactive and real power flow at each of the AC systems to which it is connected, at the Point of Common Coupling (PCC). In contrast to line-commutated HVDC transmission, the polarity of the DC voltage link remains the same with the DC current link being reversed to change the direction of power flow [5-7].

Converter stations with dc fault reverse-blocking capability (Figure 1). Each converter station must be able to block current flow between the ac and dc sides during a dc fault, thus allowing dc-side capacitor discharge current, which is the major component of the dc fault current, to decay to zero and then isolate the fault.

Figure 1 shows the $\pm$230 kV, 2000 MVA AC systems (AC system1 and AC system2 subsystems) that are modeled by damped *L-R* equivalents at fundamental frequency of 50 Hz and at the third harmonic. The VSC are three-level bridges block close to an ideal switching device model of IGBT/diodes. The relative ease with which the IGBT can be controlled and its suitability for high-frequency switching has made this device the better choice over gate turn-off thyristors (GTO) [8].

3. HIGH LEVEL BLOCK DIAGRAM OF THE DISCRETE VSC CONTROLLER

Figure 2 shows the VSC Controller subsystem of 230 kV, 2000 MVA; the sample time of the controller model is 74.06 μs, which is ten times the simulation sample time. The latter is chosen to be one hundredth of the PWM carrier period (i.e., 0.01/1350 s) giving an acceptable simulation precision. The power elements, the anti-aliasing filters and the PWM Generator block use the fundamental sample time of 7.406 μs. The normalized sampled voltages and currents (in p.u.) are provided to the controller [9-10].

The Clark Transformations block transforms the three-phase quantities to space vector components α and β (real and imaginary part). The signal measurements (*U* and *I*) on the primary side are rotated by $\pm\pi\backslash 6$ according to the transformer connection (YD11 or YD1) to have the same reference frame with the signal measured on the secondary side of the transformer. The *dq* transformations block computes the direct axis *"d"* and the quadratic axis *"d"* quantities (two axis rotating reference frame) from α and β quantities [11-13].

4. PHASE LOCKED LOOP

The phase locked loop (PLL) shown in figure 3 is used to synchronise the converter control with the line voltage and also to compute the transformation angle used in the $d-q$ transformation.

The PLL block measures the system frequency and provides the phase synchronous angle θ for the d–q transformations block. In steady state $sin\,(\theta)$, is in phase with the fundamental (positive sequence) of α component and phase A of the point of common coupling voltage (U_{abc}).

5. ACTIVE, REACTIVE POWER AND VOLTAGE LOOP

The power loop control uses the well-known expressions for active and reactive power transfer where active power is related to the power transfer angle and reactive power which is related to the magnitude of the voltage. If the power transfer angle is small, the active and reactive power exhibited in Eqs. (1) and (2) can be simplified as [14-15]:

$$P = \frac{3}{2} \times Re\left(u_f^{-dq} \times i_v^{-dq}\right) = \frac{3}{2} \times \left(u_{fd}{}^{*} i_{vd} + u_{fq}{}^{*} i_{vq}\right) \quad (1)$$

$$q = \frac{3}{2} \times Re\left(u_f^{-dq} * i_v^{-dq}\right) = \frac{3}{2} \times \left(u_{fd}{}^{*} i_{vd} + u_{fq}{}^{*} i_{vq}\right) \quad (2)$$

If the reference dq-frame is selected such that the quadrature component of the voltage is very small and may be negligible $\left(u_{Lq} \approx 0\right)$ then the Eqns. (1) and (2) indicates that the active and the reactive power are proportional to the d and q component of current respectively. Accordingly, it is possible to control the active power (or the DC voltage or the DC current) and the reactive power (or the AC bus voltage) by control of the current components i_{vd} and i_{vq}. The active and reactive power and voltage loop contains the outer loop regulators that calculate the reference value of the converter current vector $\left(I_{dq}\right)$ which is the input to the inner current loop. The control modes are in the *"d"* axis either as active power flow at the point of common coupling (*PCC)* or the pole-to-pole DC voltage in the *"q"* axis. The reactive power control regulator block combines a *PI* control with a feed-forward control to increase the speed response [16-18].

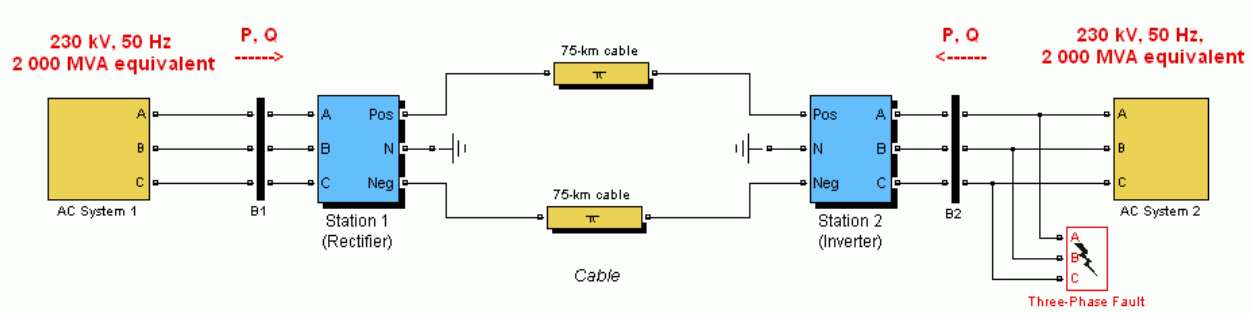


Figure 1: VSC-HVDC Transmission System Model

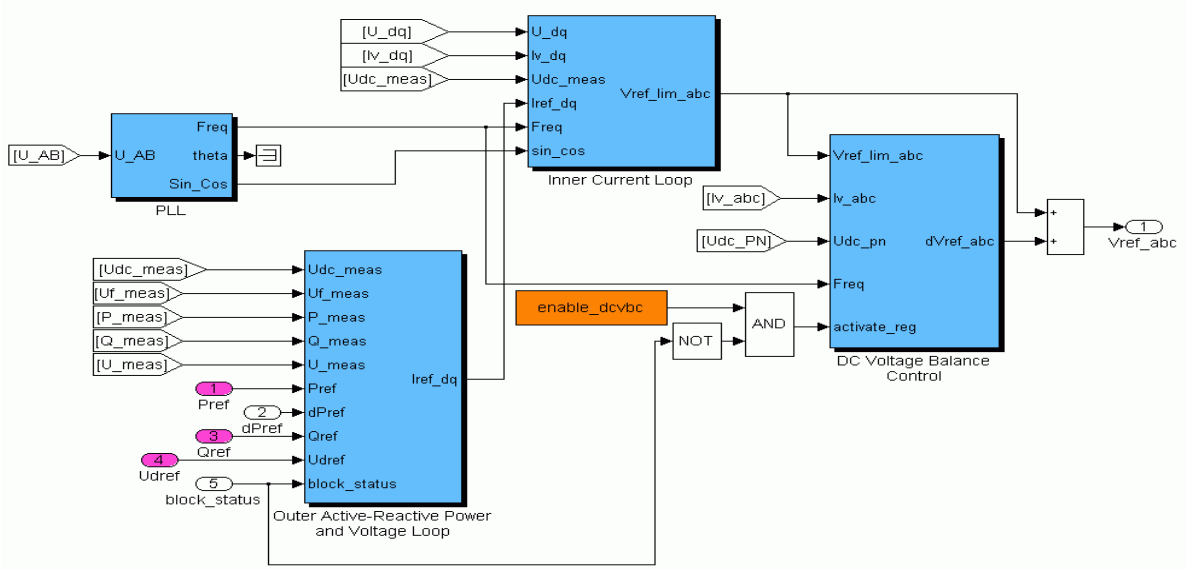


Figure 2: VSC Controller subsystem

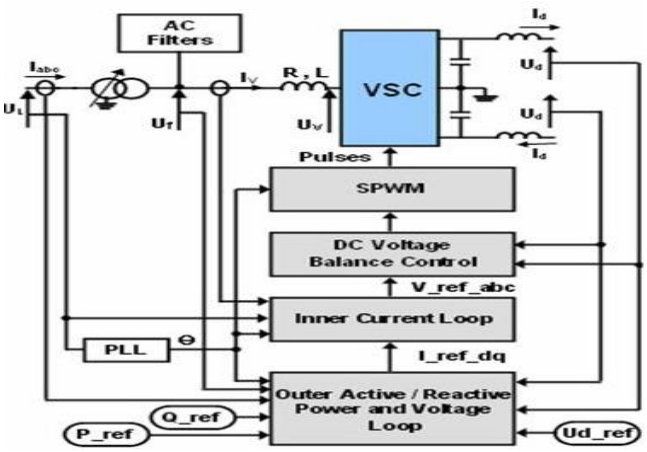


Figure 3: Overview diagram of the VSC control system

6. CURRENT LOOP

For each of the phases it can be expressed as (Figure 3):

$$u_f - u_v = L\frac{di_v}{dt} + R^* i_v \qquad (3)$$

where $u_f$is the positive and u_f is the negative sequence voltages, while $i_v$is the current and L is the inductor. The unbalanced operation of the expression for the voltage drop over the reactor $(R + j\omega L)$holds for both positive and negative-sequence voltages and currents; the voltage drop is described by the differential equation in equation (3)[19-21]:

$$\frac{d}{dt}\begin{bmatrix} i_{vaX} \\ i_{ivbX} \\ i_{vcX} \end{bmatrix} = \begin{bmatrix} \frac{-R}{L} & 0 & 0 \\ 0 & \frac{-R}{L} & 0 \\ 0 & 0 & \frac{-R}{L} \end{bmatrix} \times \begin{bmatrix} i_{vaX} \\ i_{ivbX} \\ i_{vcX} \end{bmatrix} - \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L} \end{bmatrix} \times \begin{bmatrix} i_{vaX} \\ i_{ivbX} \\ i_{vcX} \end{bmatrix} \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L} \end{bmatrix} \times \begin{bmatrix} i_{vaX} \\ i_{ivbX} \\ i_{vcX} \end{bmatrix} \qquad (4)$$

where $X = (p)$ for positive sequence and (n) for negative sequence. Eqn. (4) can be transformed to α -β-frame; this gives for the voltages and currents as:

$$\frac{d}{dt}\begin{bmatrix} i_{vaX} \\ i_{\beta X} \end{bmatrix} = \begin{bmatrix} \frac{-R}{L} & 0 \\ 0 & \frac{-R}{L} \end{bmatrix} \times \begin{bmatrix} i_{vaX} \\ i_{\beta X} \end{bmatrix} - \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \times \begin{bmatrix} i_{vaX} \\ i_{\beta X} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \times \begin{bmatrix} i_{vaX} \\ i_{\beta X} \end{bmatrix} \qquad (5)$$

Eqn. (5) can be further transferred into the rotating *dq*-frame as:

$$\frac{d}{dt}\begin{bmatrix} i_{vdX} \\ i_{dX} \end{bmatrix} = \begin{bmatrix} \frac{-R}{L} & \omega \\ -\omega & \frac{-R}{L} \end{bmatrix} \times \begin{bmatrix} i_{vdX} \\ i_{dX} \end{bmatrix} - \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \times \begin{bmatrix} i_{vdX} \\ i_{dX} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \times \begin{bmatrix} i_{vdX} \\ i_{dX} \end{bmatrix} \quad (6)$$

And

$$\frac{d}{dt}\begin{bmatrix} i_{vdn} \\ i_{vqn} \end{bmatrix} = \begin{bmatrix} \frac{-R}{L} & \omega \\ -\omega & \frac{-R}{L} \end{bmatrix} \times \begin{bmatrix} i_{vdn} \\ i_{vqn} \end{bmatrix} - \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \times \begin{bmatrix} i_{vdn} \\ i_{vqn} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \times \begin{bmatrix} i_{vdn} \\ i_{vqn} \end{bmatrix} \quad (7)$$

The positive and negative sequence voltages of the VSC side are obtained from (6) and (7):

$$U_{vdp} = U_{fdp} - R^* i_{vdp} + \omega L\, ^* i_{vqp} - L\frac{d}{dt} i_{vdp} \quad (8)$$

$$U_{vqp} = U_{fqp} - R^* i_{vqp} + \omega L\, ^* i_{vdp} - L\frac{d}{dt} i_{vqp} \quad (9)$$

And

$$U_{vdp} = U_{fdp} - R^* i_{vdp} + \omega L\, ^* i_{vqn} - L\frac{d}{dt} i_{vdn} \quad (10)$$

$$U_{vqp} = U_{fqp} - R^* i_{vqp} + \omega L\, ^* i_{vdn} - L\frac{d}{dt} i_{vqn} \quad (11)$$

The mean voltages over the sample period k to $k+1$ are derived by integrating (8), (9), (10) and (11) from kT_s to $(k+1)T_s$ and dividing by T_s (where T_s is the sampling time).

$$\bar{U}_{vdp} = \bar{U}_{fdp} R^* i_{vdp} + \omega L\, ^* i_{vqp} - \frac{L}{T_s}\{i_{vdp}(k+1) - i_{vdp}(k)\} \quad (12)$$

$$\bar{U}_{vqp} = \bar{U}_{fqp} R^* i_{vqp} + \omega L\, ^* i_{vdp} - \frac{L}{T_s}\{i_{vqp}(k+1) - i_{vqp}(k)\} \quad (13)$$

And

$$\bar{U}_{vdu} = \bar{U}_{fdu} R^* i_{vdn} + \omega L\, ^* i_{vqn} - \frac{L}{T_s}\{i_{vdn}(k+1) - i_{vdn}(k)\} \quad (14)$$

$$\bar{U}_{vqn} = \bar{U}_{fqn} R^* i_{vqn} + \omega L\, ^* i_{vdn} - \frac{L}{T_s}\{i_{vqn}(k+1) - i_{vqn}(k)\} \quad (15)$$

By assuming linear current and constant network voltage (the network voltage varies very little during a switching time period) during one sample period T_s we obtain from (12) through (15):

$$u_{vdp}(k+1) = u_{fdp}(k) - \frac{R}{2}\{i_{vdp}(k+1) + i_{vdp}(k)\} + \frac{\omega L}{2}\{i_{vqp}(k+1) = i_{vqp}(k)\} - \frac{L}{T}\{i_{vdp}(k+1) = i_{vdp}(k)\} \quad (16)$$

$$u_{vqp}(k+1) = u_{fqp}(k) - \frac{R}{2}\{i_{vqp}(k+1) + i_{vqp}(k)\} + \frac{\omega L}{2}\{i_{vdp}(k+1) + i_{vdp}(k)\} - \frac{L}{T}\{i_{vqp}(k+1) - i_{vqp}(k)\} \quad (17)$$

$$u_{vdn}(k+1) = u_{fdn}(k) - \frac{R}{2}\{i_{vdn}(k+1) + i_{vdn}(k)\} + \frac{\omega L}{2}\{i_{vqn}(k+1) + i_{vqn}(k)\} - \frac{L}{T}\{i_{vdn}(k+1) - i_{vdn}(k)\} \quad (18)$$

$$u_{vqn}(k+1) = u_{fqn}(k) - \frac{R}{2}\{i_{vqn}(k+1) + i_{vqn}(k)\} + \frac{\omega L}{2}\{i_{vdn}(k+1) + i_{vdn}(k)\} - \frac{L}{T}\{i_{vqn}(k+1) - i_{vqn}(k)\} \quad (19)$$

The control is based on (16), (17), (18) and (19), where the voltages and currents at time ($k+1$) are thus equal to the reference values at time step (*k*).

7. DC VOLTAGE BALANCE CONTROL

The difference between the DC side voltages (positive and negative) are controlled to keep the DC side of the three level bridge balanced (i.e., equal pole voltages) in steady-state. Small deviations between the pole voltages may occur at changes of active/reactive converter current or due to nonlinearity on lack of precision in the execution of the pulse width modulated bridge voltage. Furthermore, deviations between the pole voltages may be due to inherent unbalance in the circuit components impedance. The DC midpoint current Id_0 determines the difference Ud_0 between the upper and lower DC voltages (Figure. 4).Furthermore, deviations between the pole voltages may be due to inherent imbalance in the circuit components impedance. The AC current control block tracks the current reference vector ("d" and "q" components) with a feed-forward scheme to achieve a fast control of the current at load changes and disturbances. The state equations representing the dynamics of the VSC currents are used (an approximation is made by neglecting the AC filters). The

"q" and *"d"* components are decoupled to obtain two independent first-order plant models. A proportional integral (*PI*) feedback of the converter current is used to reduce the error to zero in steady state [22-24].

The ratio between the maximum fundamental peak phase voltage and the DC total voltage (i.e., for a modulation index of 1) is $(\sqrt{2}/\sqrt{3}) = 0.816$. By choosing a nominal line voltage of 100 kV at the transformer secondary bus and a nominal total DC voltage of 200 kV the nominal modulation index would be 0.816. The converter should be able to generate up to $1/0.816$ or 1.23 p.u when the modulation index is equal to 1. This voltage margin is important for generating significant capacitive converter current (i.e., a reactive power flow to the AC system).

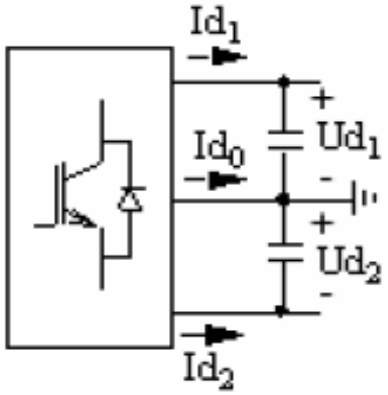


Figure 4: DC Voltages and Currents of the Three-Level Bridge

$$Id_0 = -(Id_1 + Id_2) = -C\frac{d}{dt}(Ud_1 - Ud_2) = -C\frac{d}{dt}(Ud_0) \quad (20)$$

In (20), Ud_1 and Ud_2 are average voltage while Ud_0 is the difference voltage and Id_0 is the current.

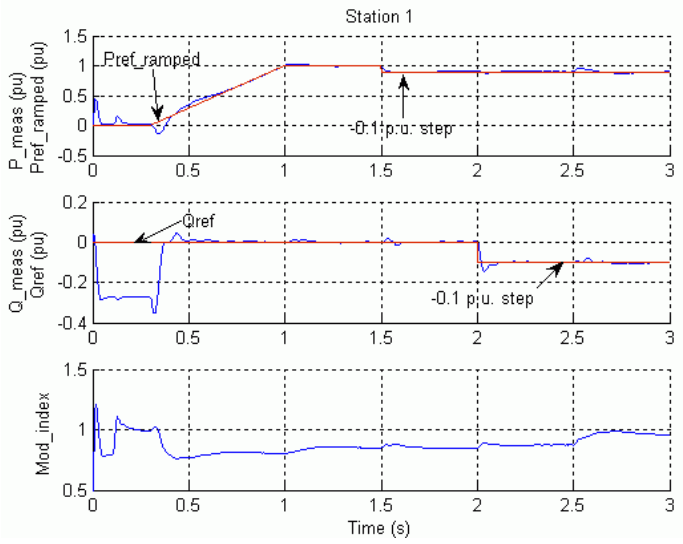
From Figure 4, the DC voltage balance control conduction time of the switches can be enabled or disabled. The difference between the DC side voltages (positive and negative) that is the average voltage Ud_1 and Ud_2 of the DC midpoint current Id_0 thus thereby controlling the difference voltage Ud_0 are controlled to keep the DC side of the three level bridge balanced (i.e., equal pole voltages) in steady-state. A positive difference ($Ud_0 \geq 0$) can be decreased to zero if the amplitude of the reference voltage which generates a positive midpoint current is increased at the same time as the amplitude of the reference voltage which generates a negative DC Small deviations between the pole voltages may occur at changes of active/reactive converter current or due to nonlinearity on lack of precision in the execution of the pulse width modulated bridge voltage. Consequently, the bridge voltage becomes distorted thus; to limit the distortion effect the control can be done slowly by activating the station controlling the DC voltage [25-26].

8. DYNAMIC PERFORMANCE SIMULATION USING MATLAB/SIMULINK

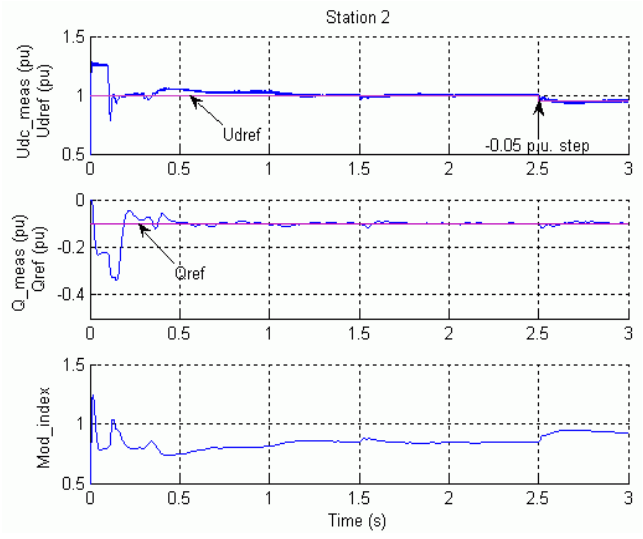
The dynamic performance of the transmission system is verified by simulating and observing the

- Dynamic response to step changes applied to the principal regulator references, like active/reactive power and DC voltage
- Recovery from minor and severe perturbations in the AC system

Simulation is carried out using Figure 1.Station 2 converter controlling DC voltage is first deblocked at t = 0.1 s. Then, station 1 controlling active power converter is deblocked at t = 0.3 s and power is ramped up slowly to 1 p.u. Steady state is reached at approximately t =1.3 s with DC voltage and power at 1.0 p.u (230 kV, 200 MW). Both converters control the reactive power flow to a null value in station 1 and to 20 MVAR (-0.1 p.u) into station 2 system. The results obtained from the simulation are shown in Figure 5 (a) and (b).



(a) System Startup –Step Response in Station 1



(b) Steady-State and Startup and U_{dc} Step Response in Station 2

Figure 5: The main waveforms from the scopes are reproduced below.

9. AC SIDE PERTURBATIONS

From the steady-state condition, a minor but severe perturbation is executed at Stations 1 and 2 systems respectively (see Figure 1). A three-phase voltage sag is first applied to Station 1 bus. Then, following the system recovery, a three-phase to ground fault is applied to station 2 bus. The system recovery from the perturbations should be prompt and stable. The main waveforms from the scopes are reproduced in the two Figures (6) and (7).

10. FAST FOURIER TRANSFORM ANALYSIS

The principal harmonic voltages are generated at and around multiples of *p*. The shunt AC filters are 27th and 54th high pass totaling 40 MVAR. To illustrate the AC filter action, we did an FFT analysis in steady state of the converter phase A voltage and the filter bus phase A voltage, using the Powergui block. The results are shown in Phase A Voltage and FFT Analysis: (a) Converter Bus (b) Filter Bus.

Thus, to meet AC system harmonic specifications, AC filters forms an essential part of the scheme. They can be connected as shunt elements on the AC system side or the converter side of the converter transformer. Since there are only high frequency harmonics, shunt filtering is therefore relatively small compared to the converter. With the arrangement of a converter reactor or air cored device which separates the fundamental frequency (filter bus) from the raw PWM waveforms (converter bus), a high pass filter is sufficient thus, no tuned filters are needed.

Figure 8 (a) and (b) shows the analysis of the Voltage waveform and FFT wave spectrum, the DC side filters blocking high-frequency are tuned to the 3rd harmonic, i.e., the main harmonic present in the positive and negative pole voltages.

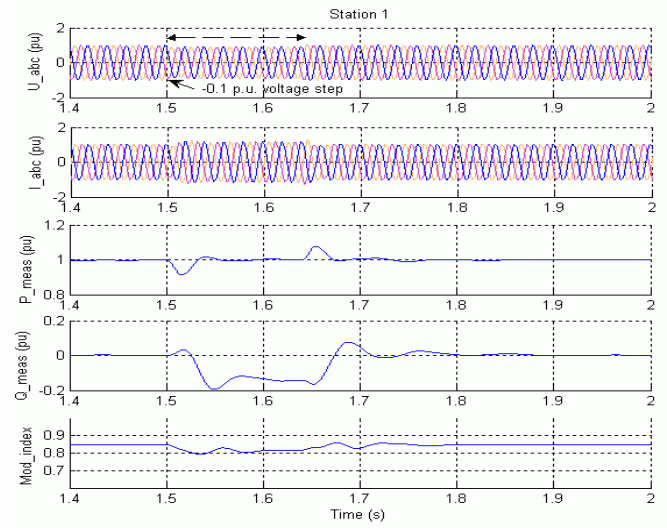


Figure 6: Voltage Step on AC System 1

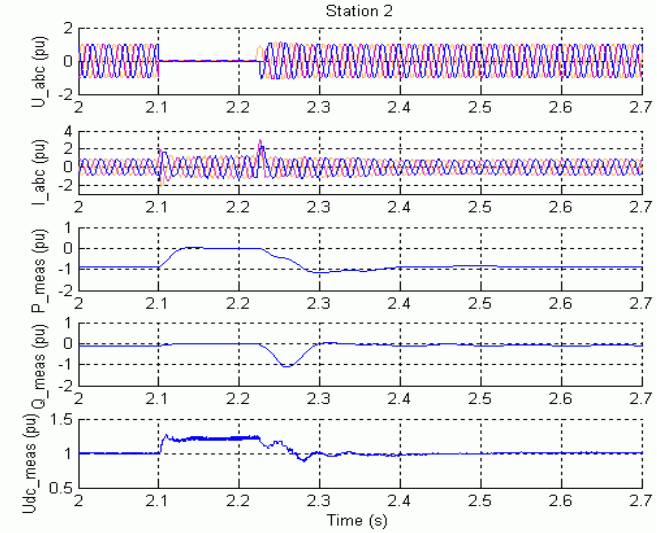
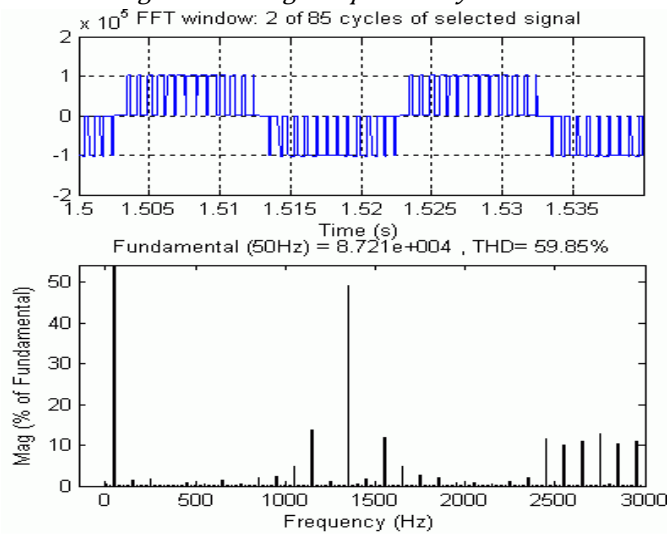
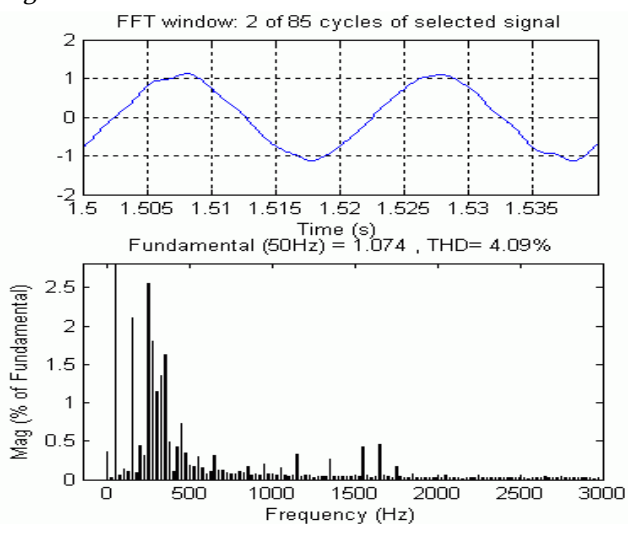


Figure 7: Three-Phase to Ground Fault at Station 2 Bus



(b)



(a)

Figure 8: Phase 'A' Voltage and FFT Analysis: (a) Converter Bus (b) Filter Bus

The reactive converter current generates a relatively large third harmonic in both the positive and negative pole voltages but not in the total DC voltage. To keep the DC side balanced, the level of the difference between the pole voltages has to be controlled and kept to zero. The rectifier and the inverter are interconnected through a 75 km cable (2 pi sections).

11. CONCLUSION

In this paper, recent advances of the VSC-HVDC technology are presented. The use of power electronic in HVDC with a number of key benefits namely independent control of active and reactive power through the control of the converter. The simulation results of active and reactive power of system show the successful power transmission by VSC-HVDC link using the VSC-based HVDC technology systems at voltage levels up to $\pm$230 kV and power levels up to 200 MW have been established and tested by means of simulations. General guidelines for tuning the controllers are presented under simulations in Matlab/Simulink environment.

From the simulation, it can be seen that the VSC-HVDC can fulfill fast and bi-directional power transfers. Furthermore, single-phase fault the transmitted power can be kept constant except a small oscillation during the fault. However, during a three-phase fault; the decreased voltage at the converter terminals strongly reduces the power flow by the DC link. When the fault is cleared, normal operation is recovered fast.

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