DESIGN AND CONSTRUCTION OF AN INFRARED ACTIVATED ENTRANCE AND EXIT COUNTING DEVICE

A. S. Adekola, A. M. Arogunjo, K. D. Adedayo and S. B. Eniafe
Department of Physics, Federal University of Technology, P. M. B. 704, Akure, Nigeria

Abstract. This paper presents the design procedure and construction of a low powered entrance and exit counting device. It uses infrared activated transmitter and receiver. The particular circuits that have been employed have been constructed using available components. The counter is capable of counting solid objects to a maximum value of nine thousand nine hundred and ninety nine.

1. INTRODUCTION

Counting is essential to our existence as human beings. Human beings have been involved in counting immediately he/she knows his/her left hand from the right. Manufacturing companies will want to know the number of items they can afford to produce on daily basis so as to be able to predict the production capacity of their machine. Porters at the entrance of a library are interested in knowing the number of library users already in the library so as to be able to predict the remaining space available. In a vehicle garage, a thorough monitoring and control system is needed, as to be able to know the number of vehicles the garage can still accommodate.

Counting becomes a burden and uninteresting when what to count is enormously large. This project therefore finds its application in any system that involves counting in an attempt to predict the capacity of such system. The system will not only display a sequential increase in what is entering, the same display will give us the net number whenever there is an exit.

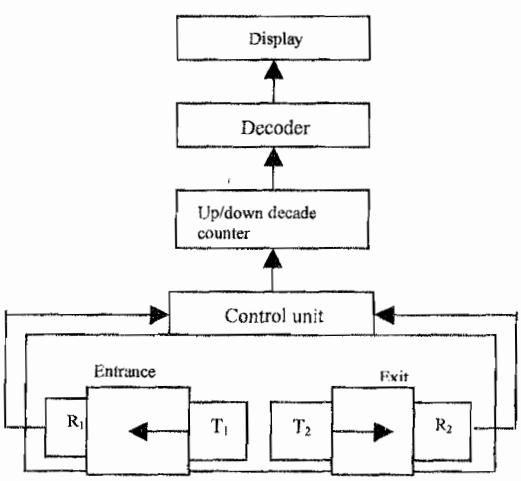

Fig.1: block diagram of the infrared activated entrance and exit counting device

Nig. J. Pure Appl. Phys. (2003) Vol.2 pp 54 - 58. Printed in Nigeria, ISSN 1596-0862. E-mail: njpap@futa.edu.ng. For rights of reproduction and web access, contact African Journals Online, UK, www.inaps.ajol

2. THE DESIGN PROCEDURE AND OPERATION OF VARIOUS UNITS

Fig 1 shows the block diagram of the project. T1 and R1 are infrared transmitter and receiver respectively, which are expected to be installed at the entrance while T2 and R2 are the infrared transmitter and receiver respectively, which are expected to be installed at the exit. The design procedure and operation of various units are hereby presented.

The control unit consists of 555 timers IC1 - IC3. Their arrangement is presented in Fig 2. Each of the timers is connected as a one-shot multivibrator. IC1 generates the up count pulses while IC3 generates the down count pulses.

Without a trigger pulse, pin 7 (Dis) of each of the timer will be almost at zero volts, the output pin 3 of IC2 will be low hence capacitor C1 cannot be charged. When a negative-going triggering pulse (high to low digital signal) is applied, the output switches to Vcc volts. C1 begins to charge via R1 so that the voltage across it rises exponentially towards Vcc. When this voltage exceeds 2/3 of Vcc, the output switches to zero volt. The width of the output device is equal to the time T taken for the external capacitor C1 to charge from zero to 2/3Vcc [1] expressed as

$$T = 1.1\ C1\ R1 \qquad (1)$$

R1 can be of minimum value 1 kΩ and maximum value of 13 MΩ. This is to satisfy the condition of generating the trigger pulse as reported by Douglas [1]. In practice however, medium values of R1 ranging from 50 KΩ to 1 MΩ have been recommended by Douglas [1] and Bogart [2]. R1

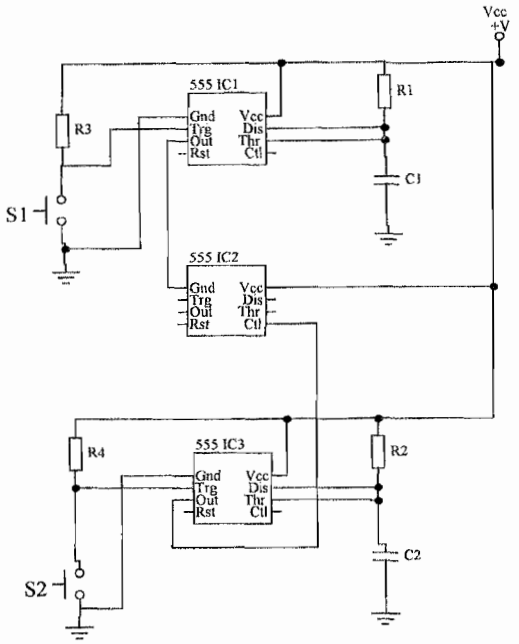

Fig 2: Circuit diagram of the control unit

has been selected to be 1 MΩ and this assumes a minimum time of 0.5 seconds at which two successful and close objects can be counted. Using eqn (1) therefore, the value of capacitor C1 is calculated to be 0.45 μF.

A synchronous counter, which is an arrangement of flip-flops and logic gates, has been used in this work. It has advantages over the asynchronous type in that it does not suffer false states during its output sequence and the cumulative propagation delay of the counting is eliminated. The particular type of synchronous counter that has been used in this work is the 74192 IC because of its outstanding characteristics over others [2]

- it can be cascaded easily without any additional circuitry.
- it is a synchronous reversible counter. This assists in eliminating the output counting spikes that are usually associated with asynchronous counters.
- the output of the counter can be preset to either HIGH or LOW level.

The combined circuit diagram of the up/down decade counter, decoder and the display is shown in Fig 3. The inputs count up (pin 5) and count down (pin 4) are triggered by a low-high transition clock input from the control unit. The direction of counting is determined by the count input that is pulsed while the other count input is high that is for counting up, the count down must be held high and the clock signal applied to the count up input or the other way round.

The outputs from the up/down counter are fed into their respective decoder. A decoder is an interface that converts BCD information from the up/down counter to decimal information. It is meant to translate the 8421 BCD code to a seven-segment display code that lights the segments of the display. The particular decoder that has been employed in this work is TTL 7447, which is commonly used in the design of digital counter (R) as presented in Fig 3, to give a maximum count of nine thousand, nine hundred, and ninety-nine. Further cascading gives higher digit of counting. The counting sequence can be read on the display, which is a seven-segment display. When the clock signals are applied to the count up, the sequence increases numerically. However if clock signals are applied to the count down, the sequence decreases numerically. Resistors R7 – R34 are current limiting resistors, which range between 150 and 500 Ω since the forward voltage drop across LED is typically 1.6 V [3].

The transmitter consists of a 555 timer connected in the astable mode (see Fig 4). Pins 2 and 6 are connected together so as to allow capacitor C5 to charge and discharge between the threshold and trigger levels. When the Vcc is connected, C5 charges through R35 and R36. When the voltage across C5 reaches 2/3Vcc, the output changes state and C5 is discharged through R36 towards zero volts. When this voltage (across C5) falls to 1/3Vcc, the circuit again changes state, the internal discharge transistor turns off and C5 begins to charge again. Thus a continuous train of pulses appears at output pin 3, in which its period T is given as [4]

$$T = C5\,(R35 + 2R36)\ln 2 \qquad (2)$$

The transmitter has been designed to transmit the infrared signal at a frequency of 9 KHz. This falls in the very low frequency (VLF) range of the electromagnet spectrum. This frequency is suitable for standard frequency emissions and has strong penetration depth [5]. For a pulse of 0.11 mS therefore, a low valued capacitor C5 has been recommended [6]. The value of C5 chosen for this work is 1.0 μF with R36 equal 39 kΩ. Using eqn (2), the value of R35 has been calculated to be 82 KΩ. The output of the astable multivibrator at pin 3 consists of a pulse stream, which is fed into a constant-current source TR1. This source provides the infrared transmitting diode D3 with appropriate current that activates it for continuous emission of infrared signal. The quiescent dc base voltage, V_B is given by

$$V_B = V_{D1} + V_{D2} \qquad (3)$$

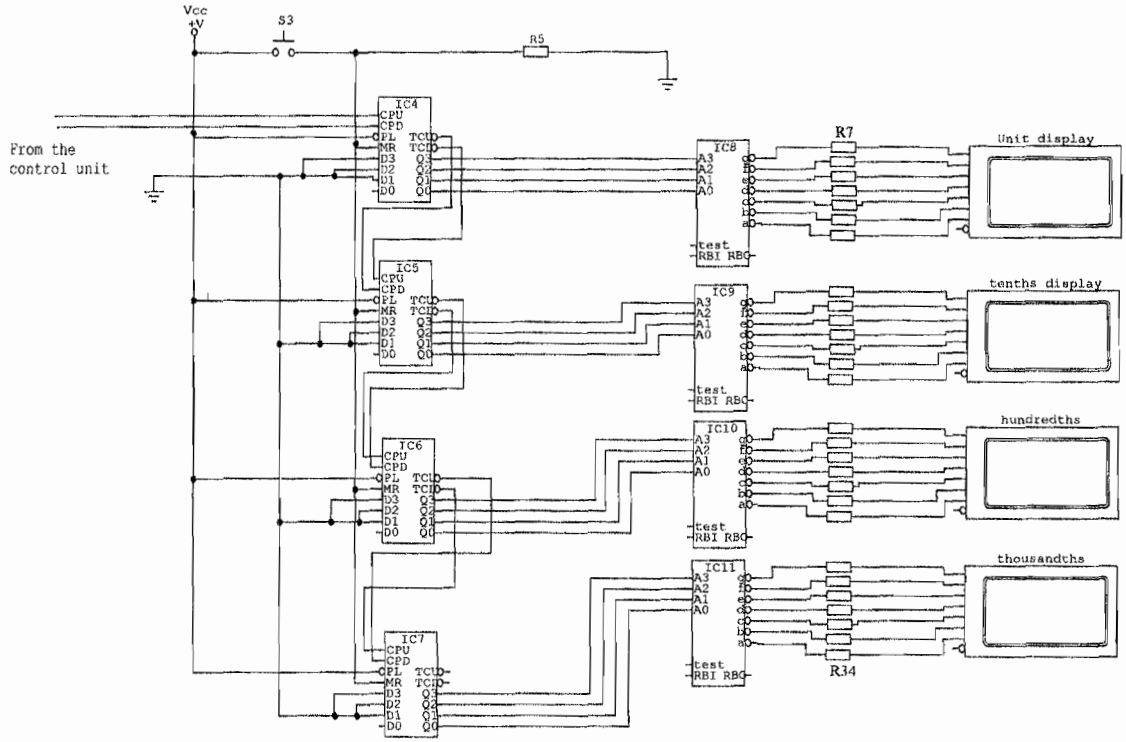

Fig.3: Combined circuit diagram of up/down decade counter, decoder and the display circuit

where V_{D1} and V_{D2} are the voltage drop across diodes D1 and D2 respectively and the value is typically 0.6 V. Also quiescent dc emitter voltage V_E is given by

$$V_E = V_B - V_{BE} \quad (4)$$

where V_{BE} is the base-emitter voltage of the TR1 and the value is typically equal to 0.8 V. Hence, using eqns (3) and (4), V_E is calculated to be 0.4 V. The quiescent collector current, I_C is therefore given by

$$I_C = \frac{V_E}{R38} \quad (5)$$

A maximum current of 100 mA is recommended to flow through the infrared emitter for efficient radiation [1]. Using eqn (5) therefore gives the value of R38 as 4 Ω.

The major component of the infrared receiver is the LM392N IC shown in Fig 5. The IC contains a precision voltage comparator and an Op-amp in an 8-pin DIL package. TR2 is the phototransistor, which receives the pulsating infrared light and amplifies it, hence it forms a cascaded amplifier with TR3. This arrangement ensures that the amplified output signal is in phase with the coming pulsating signal.

The combination of capacitor C9 and C10, diodes D4 and D5 and resistor R45 forms both a voltage doubler so as to double the output voltage and rectifies the pulsating output signal from pin 7. When the non-inverting voltage at pin 3 is higher than the inverting voltage at pin 2, the comparator produces a high output voltage at pin 1. When the non-inverting input is less than the inverting input, the comparator produces a low input voltage. The logic level at pin 1 remains HIGH as long as TR2 receives the pulsating infrared light. This is fed to the drive transistor TR5 and energizes the relay, thereby making S1 in the control unit to open and pin 2 of IC1 will be at logic 1. When the pulse stream between the infrared transmitting diode D3 of Fig 3 and TR2 of Fig 3 is broken, the logic level at pin 1 of the LM392N IC goes low and the relay is de-energized and this caused S1 to close and the logic 1 at pin 2 of IC1 to go to logic 0, thereby generating a triggering pulse. The counter then counts these pulses.

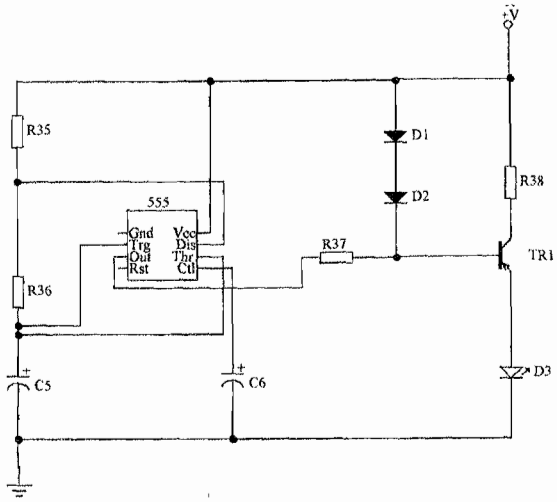

Fig 4: Circuit diagram of the infrared transmitter.

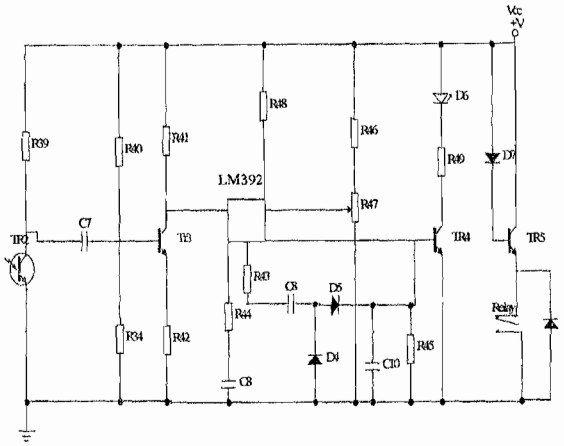

Fig.5: Circuit diagram of the infrared receive

(LM392 is an integrated circuit)

The power supply unit is a source of stable dc voltage for the entrance and exit electronic counter. It consists of a 6 V transformer, two bridge rectifiers, filters and voltage regulator. The type of voltage regulator used in this work is a 3-terminal transistorized regulator 7805 IC that has a fixed output of 5 Vdc and 7809 IC with a fixed output of 9 Vdc.

The infrared receiver receives pulsating infrared light from the transmitter, which continuously emit infrared signal. When this pulse stream is broken either at the entrance or exit, it causes IC1 to generate up count pulses for the entrance circuit and down count pulses for the exit circuit. The inputs count up and count down of the decade counter is triggered by the transition inputs from the control unit. The direction of counting is determined by the count input that is pulsed.

3. TESTING AND CONCLUSION

The various units that have been described were coupled using flexible wires. The transmitter and receiver were placed at a distance not more than 2 m apart. This ensures one solid object to pass through the entrance or exit where the transmitters and receivers are placed. The photographs of the internal circuitry and pictorial view of the complete entrance and exit counter are presented in Figs 6 and 7 respectively.

This paper has presented the design procedure and construction of entrance and exit electronic counter. The particular circuit diagrams that have been adopted for this work are also presented. Various advantages of some of the components used in this work were also highlighted. The configuration of the decoders used in this work gives a maximum count of nine thousand, nine hundred, and ninety-nine. The list of all the components used in this work is presented in the appendix. The work would be an invaluable tool for manufacturing companies, libraries, conferences and car parks.

Acknowledgement

The authors wish to thank the Department of Physics, Federal University of Technology, Akure, Nigeria for providing some of the electronic components used in this work.

REFERENCES

1. Douglas, V. H. (1989): Digital Circuits and Systems. Mc-Graw Hill NY, p 239 – 240
2. Bogart, T. (1980): Electronic Devices and Circuits. Oxford University Press, England, p 500 – 510.
3. Maddock, R. J. and Calcutt, D. M. (1988): Electronic, A course for Engineer. Longman, p 301 – 302
4. Tokhem, D. (1980): Digital circuits. John Wiley, NY.p 71 – 105
5. Hall, M. P. H and Barclay, L. W. (1989) Radiowave propagation. Peter Peregrinus Ltd, UK. p 278
6. Millman, J. and Halkias, C. C. (1974): Integrated electronics. McGraw Hill Int NY.p P 624

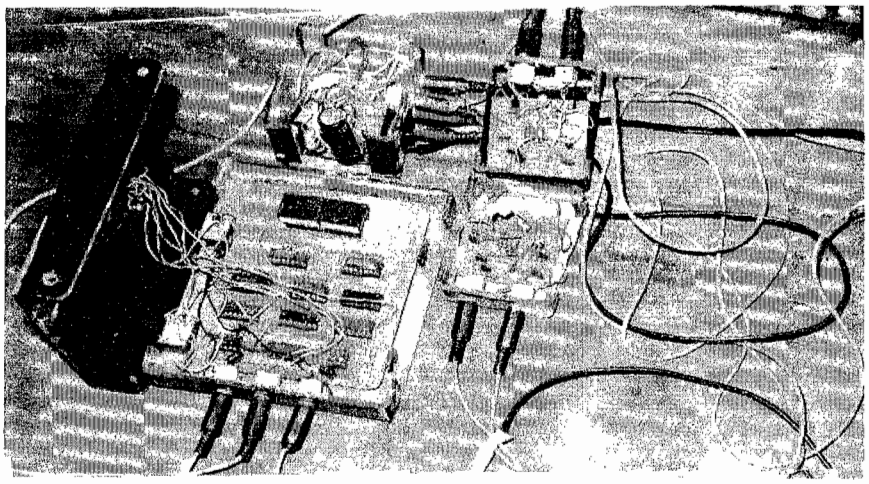

Fig 6: Photograph of the internal circuitry of the infrared activated entrance and exit counting device

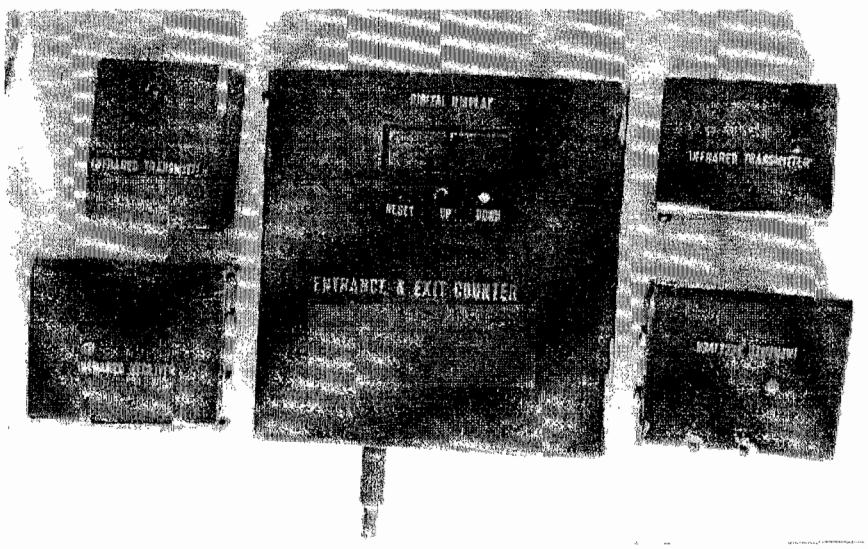

Fig 7: Pictorial view of the infrared activated entrance and exit counting device

Appendix: List of all the electronic components

Resistors	Capacitors	Integrated circuit	Transistors	Diodes
R1 = R2 = 1 MΩ	C1 = C2 = 0.45μF	IC1 – IC3 = 555	TR1 = BC559	D1 – D4 = IN4148
R3 = R4 = 470 Ω	C5 = C6 = 1 μF	IC4 – IC7 = 74192	TR2 = Photo-transistor	D3 = Infrared emitter
R7 – R34 = 220 Ω	C7 – C10 = 10 nF	IC8 – IC11 = 7447	TR3 = BC337	D5 = OA91
R35 = 82 KΩ	C11 = 1000 μF	IC13 = LM 392	TR4 = 2SC945	D6 = LED
R36 = 39 KΩ	C12 = 10 μF		TR5 = BC337	D7 = D8 = IN4001
R37 = R38 = 3.9 KΩ				
R39 = 470 KΩ				
R40 = 100 KΩ				
R41 = 2.7 KΩ				
R42 = 100 KΩ				
R43 = 22 KΩ				
R44 = 1 KΩ				
R45 = 10 KΩ				
R46 = 2.7 KΩ				
R47 = 5 KΩ				
R48 = 1 KΩ				
R49 = 220 KΩ				