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Performance of Concatenated Single Parity Bit Coding Along and Across Track in TDMR Media

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Research Article

Abstract

This paper presents two coding approaches of concatenated single parity codes together with their implementation and performance evaluation. The first approach uses two concatenated single parity bit codes along the track direction separated by a Dithered relative prime (DRP) interleaver. While the second approach uses the two single parity bit codes in both along and across track directions without interleaving. The results obtained for situations of high inter-symbol interference (ISI) and inter-track interference (ITI) show a better performance with the former approach as against the latter applied in a two-dimensional magnetic recording media (TDMR).

Keywords
2D detection; 2D equalization; Bahl Cocke Jelinek Raviv algorithm; Dithered relative prime; interleaver, Parity-check coding;

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1. Introduction

The widespread dissemination of internet activities, online streaming services, cloud computing and big data application have pushed the amount of user data generated to an unprecedented high. This amount is expected to reach up to 163 Zettabytes (Zettabyte is trillion gigabytes) globally by the year 2025 as forecasted by the International Data Corporation (IDC) (Reinsel *et al.*, 2017). To keep up with the data demand, more storage capacity is needed to be shipped across all media storage which translate to an exponential increase in the capacity of the media devices.

Magnetic HDDs are among the most dominant and important storage devices over the years due their reliability and low cost per gigabytes of data. They provide a much faster, easier, denser, affordable and more portable means of storing data. The continuous demand for high-capacity data storage has pushed the areal density growth of the magnetic HDDs to an unprecedented level fast approaching the superparamagnetic limit (Guan *et al.*, 2014). In order to continue with the areal density growth beyond the limit for conventional media, researchers have developed various technologies. The proposed magnetic recording technologies includes: heat assisted magnetic recording (HAMR), bit pattern magnetic recording (BPMR), shingled write-magnetic recording and two-dimensional magnetic recording (TDMR) (Shiroishi *et al.*, 2009).

Among the candidate technologies, TDMR is an attractive proposition toward achieving the immediate areal density growth expansion because it does not require any aggressive change from the convention magnetic media. Therefore, can readily be implemented on the current conventional media with modification to the read-head and the writing process. SMR writing combined with 2D read-back signal processing techniques is employed in the TDMR system to achieve high areal density up to 10Tb/in^2 (Shiroishi, 2009). This is achieved by eliminating the guard bands between tracks to squeeze data so that data bits are written in overlapping shingles, such that the previously written bits are overwritten by the neighboring bits around them. This brings the data bits closer together and the interaction between the data bits generate severe interference in both along track and across tracks direction (Chen and Srinivasa, 2013). Therefore, advanced 2D signal processing techniques for coding, equalization, decoding and detection are needed for large scale future deployment of the TDMR technology.

Current state of the art signal processing techniques for TDMR channel employed the use low density parity check (LPDC) codes coupled with 2D equalizers and full 2D maximum likelihood (ML) detectors. The shortcoming of theses algorithms is their computational complexity especially with regards to the ML detector which is exponential with respect to the number of bits involved. And also, the sub-optimal performance of iterative decoding of LDPC codes due iterative decoding. Another drawback is of complex encoding for normally good codes.

Consequently, many researches have proposed various coding and 2D detection/detection techniques for TDMR channel. The use of a linear equalizer to cancel the interference in one direction and partial response maximum likelihood (PRML) detector in the other direction was proposed in (Muhammad *et al.*, 2015). In (Zheng *et al.*, 2014) full 2D soft output Viterbi algorithm (SOVA) detector was

employed for full signal detection. On one hand, while the use of linear equalizer reduces the complexity of signal detection, it suffers loss of performance is severe interference conditions. One the other hand full 2D SOVA gives very good performance but at the expense of high detection complexity.

A joint Viterbi detector decoder (JVDD) was proposed in (Chan *et al., 2014*) and (Shafiee *et al.,* 2015) that evades the iterative decoding process and the sub-optimality of the sum product algorithm (SPA) decoder, by combining both detection and decoding on a single trellis structure. This was done through metric thresholding and parity checking on survivor paths simultaneously, in an attempt to return the sequence with the minimum metric legal codeword. The major drawback of this approach is that the survivor paths grow exponentially as the JVDD algorithm progress leading to high computational complexity for longer codewords. In (Almustapha *et al.,* 2016) a concatenated single parity bit system, coupled with a constrained maximum a posteriori (MAP) joint detector decoder for improving the performance of magnetic recording channel was proposed. A good coding gain with reasonable complexity was achieved for 1D interference channel.

In this paper, earlier works presented in (Almustapha, *et al.,* 2016a) and (Almustapha, *et al.,* 2016b) are extended to a TDMR system with 2D interference channel. Two coding approaches using two concatenated single parity bit system for 2D interference TDMR channel were introduced and also presented. The approaches exploit the simplicity of decoding single parity bit to achieve a remarkable coding gain with reasonable complexity.

The rest of the paper is organized as follows. Section II presents the data generation and coding schemes used for this work. In section III, an overview of the TDMR channel model and equalization technique employed is discussed. The 2D MAP joint detection and decoding scheme proposed in this work is presented in Section IV. Simulation results and discussions are presented in Section V and the summary and conclusions are presented in Section VI.

2. Overview of coding, channel and detector

2.1 Data Encoding

Figures 1 and 2 depict the block diagrams of the systems under study using the proposed parity bit coding approaches. In the first approach of Figure 1, the two parity bits are applied in the along-track direction and are separated by a DRP interleaver. The information bits to be saved on the disk are first encoded by adding a single parity bit to the data to generate a single parity check code. The code appends a parity bit for every three (3) consecutive bits of data based on the odd parity check constraint. The choice of the odd parity is to serve as a run length limited (RLL) code for the media. A previous investigation shows that separating the first and second parity bits with a DRP interleaver improve performance (Crozier *et al.,* 2001).

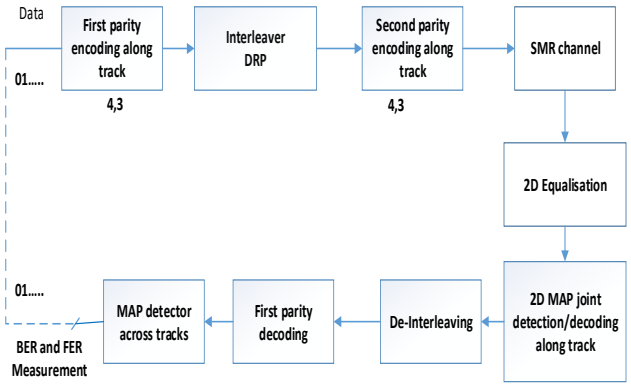

Figure 1: 2D multi-track MAP joint detector decoder with parity bits along track only

The DRP interleaver was implemented in three stages using the equations (1)-(3). The first stage called the read dither, involves randomising the bits positions locally using a small read dithered length R using eqn (1). While second stage of the interleaver involves randomising the bit positions across the whole length of the data with eqn (2). Finally, a local write dither of length W is used to randomise the bits position locally similar to the read dither using eqn (3). In our implementation, R is chosen as 8 to be 8-bit length while L is set as 3072 which is the total data bits per track after adding the first parity bits.

$$j = R\lfloor i/R \rfloor + [(m + n*i) \bmod R] \quad (1)$$

$$j = (m' + b'*i) \bmod L \quad (2)$$

$$j = W\lfloor i/W \rfloor + [(s + p*i) \bmod W] \quad (3)$$

where $\lfloor \ \rfloor$ denotes the floor(x) function, while m, n, m', b', s and p, are integer constant less than R and W respectively. is the interleaver length and is a multiple of both R and W. Also, n, b',and p are chosen relative primes. The "mod" denotes modulo division.

A total of 2304 bit per track was initially generated before adding the first parity bit. This result in a total of 3072 bits per track after the first parities are added along track. The row of 3072 data bits is randomised using the DRP interleaver. After interleaving, another single parity bit is added to a data block length of 3 along track again, using odd parity check constraint. This produced a total of 4096 bits of data per track which will be recorded on the SMR media.

For the second coding approach Figure 2, the single parity bits are used in both along-track and across-track direction without the DRP interleaving. First a single parity bit is added to the information bits along track to produce a code constraint along track, and then another single parity bit is added across tracks to give the constraint across tracks. The total data bits per track were initially 3074 bits before the first parity bits are added along track. After adding the first parities, a second parity bit is then added across tracks using the same odd single parity check constraint to form the single

parity code across tracks. No interleaver is needed here because the single parity codes are used in the different directions.

Initially, the number of tracks on the sector was 6 before adding the second parity bit across track. When the parity bits are added across tracks, the total number of tracks of the sector now becomes 8. A sector of the SMR channel model used in this work has 8 tracks and 4096 bits per track. The resulting coded data is then passed onto the SMR channel for recording.

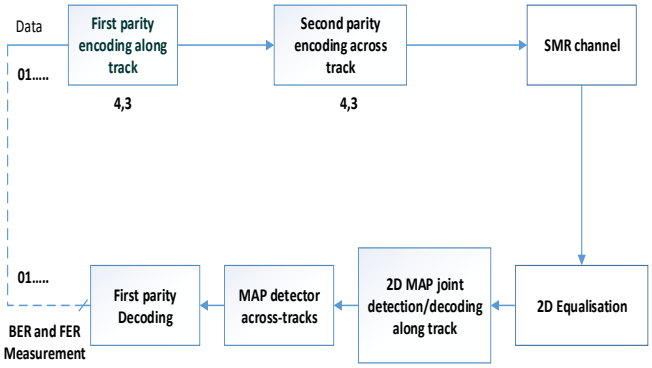

Figure 2: 2D multi-track MAP joint detector decoder with parity bits along and across tracks.

2.2 SMR Channel Modelling

SMR has the advantage of keeping the convention media structure of the magnetic recording system with some modifications to the writing and readback processes. Therefore, both ISI and ITI are of major concern and hence, ITI need to be incorporated into the channel model to account for interferences due to adjacent tracks. In conventional PMR media, the transition response for the channel S(t) can be modelled as (Hwang *et al.*, 2010);

$$S(t) = V_{\max} \tanh\left(\frac{2t}{0.579\pi T_{50}}\right) \tag{4}$$

where V_{max} is the peak signal amplitude, t is the sampling time and T_{50} is the time taken for the response to change from $-V_{max}/2$ to $+V_{max}/2$.

The dipulse response for the channel which is the isolated channel response is given by;

$$h(t-iB) = \frac{s(t-iB) - s(t-i(B+1))}{2} \tag{5}$$

Therefore, received signal from the output of a convention perpendicular magnetic recording channel (PMR) is given by Eqn. 4 as (12);

$$y(t) = \sum_i x_i h(t-iB) + \sum_i d_i a_i s'(t-iB) \tag{6}$$

Where the first term in Eqn. (6) is the convolution of the data x_i with the channel response $h(t)$ representing the data transition whereas the second term represents the first order approximation of the jitter noise.

To account for ITI due to adjacent tracks in the 2D SMR channel, Eqn (6) is modified to include data component from the preceding and succeeding tracks when reading data from the main track. Therefore, readback data (y) of any track N will have part of data component of the tracks preceding and succeeding it. Hence for any given bit position "i",

$$y_j(i) = \sum_{j=N-n_1}^{N+n_2} w_j Z_j(i) \tag{7}$$

Where w_j is the fraction of the adjacent channels contributed to the signal $y_j(i)$, n_1 and n_2 are the number of tracks preceding and succeeding the read track respectively. Also;

$$Z(t) = \sum_i x_i h(t-iB) + \sum_i d_i a_i s'(t-iB) \tag{8}$$

Therefore, the final read signal can be written by substituting (7) in (8) and representing the channel response as $h_{i,j} = w_j h(t-iB)$ and the jitter response as $s'_{i,j} = w_j s'(t-iB)$.

The received noisy signal from the 2D SMR channel output is now expressed as;

$$y_{i,j} = \sum_j \sum_i x_{i,j} h_{i,j} + \sum_j \sum_i d_{i,j} a_{i,j} s'_{i,j} + n_{i,j} \tag{9}$$

Where "i" and "j" are indexes indicating the position of the bit in the along-track and across-tacks direction respectively. With this modification in place, we have now converted the 1D PMR channel into a 2D interference channel for SMR/TDMR.

2.3 2D Equalization

In order to reduce the complexity of the detector, information signal from the channel is shaped by the equalizer to the desired target response. However, in a 2D multi-track system, two equalizers are applied in both directions for the required 2D target response to deal with interference from two directions across multiple tracks at the same time.

The equalizer coefficients required for shaping the signal to the desired target response are computed by evaluating the matrix equation expressed in (10).

$$C = H^{-1}T \tag{10}$$

where C gives the required coefficients of the equalizer, H is the matrix approximation of the channel response, and T is a column matrix formed by padding the chosen target with zeros from both sides to make it size equal to the shaping equalizer.

2.4 Maximum A Posteriori (MAP)/BCJR Detection

The MAP detection is an optimal detection technique that determines the most probable bits of data in binary (1, 0) that

are received. Unlike the ML-Sequence Detector (MLSD), which minimizes the probability of sequence error, the MAP detector tries to minimize the probability of bit error. It is a bit-wise detector that works on bit-by-bit, thus providing soft information output, which is information about the reliability of bit decision taken.

MAP detection can be implemented using the BCJR algorithm, a trellis-based detection algorithm optimized for AWGN. The BCJR algorithm uses the trellis structure and the a priori probability (branch metric) to compute the a posteriori probability (APP) of the decoded bits 1 or 0 as defined by the joint probability equation expressed in Eqn. 11 (Bahl *et al.*, 1974).

$$APP(x_i) = \sum_{s_{k-1}^{n'}, s_k^n} \alpha_{k-1}(s_{k-1}^{n'}).\beta_k(s_k^n).\gamma_k^{x_{k=i}}(s_{k-1}^{n'}, s_k^n) \quad (11)$$

The first and second terms of (11) represent the forward and backward state probabilities referred to as alpha and beta while the third term denotes the branch metrics or trellis path transition probabilities. Alpha and beta are computed recursively across the trellis section. The branch metrics (Gamma) are determined for transition from state s_{k-1} to s_k for branch "n" using Eqn. 12.

$$\gamma_k^{x_{k=i}}(s_{k-1}^{n'}, s_k^n) = \exp\left(-\frac{x_k - y_n}{2\sigma^2}\right)^2 \quad (12)$$

where x_k is the received symbol or bit at time "k", y_n is the ideal transmitted data for branch "n" at time "k", and σ^2 is the channel noise variance.

3. 2D Map Joint Signal Detection & Decoding Scheme

3.1 Multi-level/Multi-track MAP for ISI Cancellation and Single parity Decoding

The equalized readback signal from the SMR channel is passed to the multi-track 2D MAP joint signal detector decoder for joint detection and single parity decoding. BCJR algorithm is run to implement the 2D MAP joi tion and decoding of the received signal on single trell ture. For a multi-level MAP detector, the number of branch transitions per state is 2^k, while the number of state transitions is 2^{mk}. Where k is the number of bits and m is the constrain length of the detector (*Target Length-1*). In our implementation, the channel is considered to have two tracks with ITI from the main track and the side track respectively. However, due the code constraint (code length 4); target length of 4 or more is needed to perform joint detection and decoding of the equalized data. Therefore, the multi-level 2D MAP detector decoder for joint signal detection and decoding will require a trellis with 64 ($2^{3\times2}$) state transitions and 4 (2^2) incoming and outgoing branches per state.

The parity bit added to the data modifies the detector/decoder trellis such that, at the point where the parity bit enters the signal, the parity bit constraint reduces the number of branches from 4 per state to 1 branch per state in order to satisfy the parity check equation. This is because only the branches whose branch transition symbols satisfying the parity check equation are selected. As depicted by the Figure 3, the incoming parity of the signal corresponds to the bit at every fourth transition point of the trellis. For instance, it can be seen that at the fourth transition the only valid transition from state to

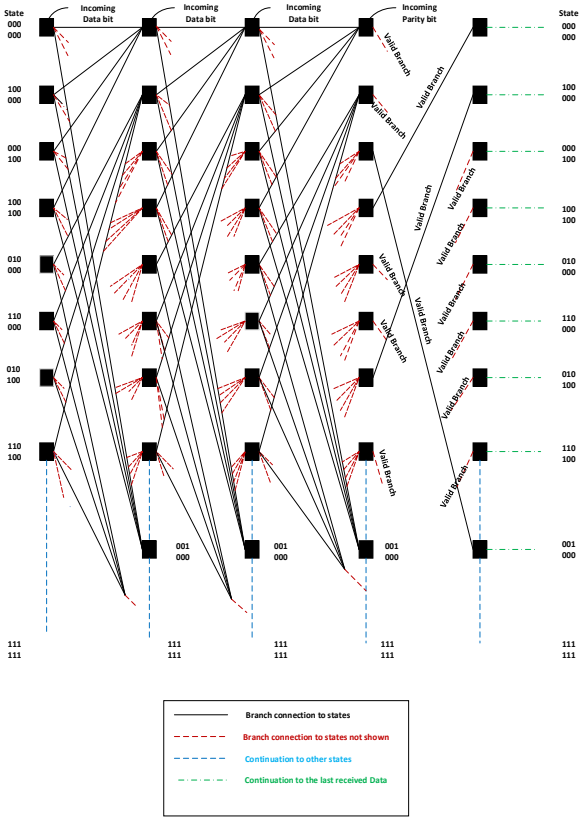

Figure 3: Trellis diagram of the 2D multi-track MAP joint detector decoder with two-track ITI

This means the component bits of the branch 000 000 which satisfy the odd parity check equation. The transition from t 000 000 o is not valid because, the branch component bits does not satisfy the odd parity check 0000 0000 . . The APP probabilities of 00, 01, 10 and 11 are determined using (11) as the output of the multi-track 2D MAP joint detector decoder. This presents a convolved soft information data across tracks with ITI from the side track. The decoded parity bits are then removed, de-interleaved and saved for the remaining signal processing processes.

3.2 Across tracks for ITI Cancellation

For the first coding approach presented, Figure 1, the across track MAP detector is employed after de-interleaving and

decoding of the first parity bits. The decoder across track uses the saved APP probabilities of 00, 01, 10, and 11 as branch metrics for computation. This APPs represents the received convoluted data across tracks with ITI from the side track. The detector runs the BCJR algorithm on a 2-state trellis with total of 4 branch transitions (2 branches per state) given by the saved APPs. The APP of the received bit being either 0 or 1 is determined to detect the data out of ITI to get the final information bits across tracks.

However, for the second coding approach, Figure 2 the across track MAP detector is employed immediately after the multi-track 2D MAP joint detector decoder. The output of the multi-track 2D MAP joint detector decoder (APP of 00, 01, 10, and 11) is fed into the across track MAP detector and is used by the detector as branch metrics. The detector across track removes the ITI from the data and the output is passed to the MAP decoder across track to decode the parity bits used across tracks. The same trellis structure is used for across track MAP detector in both the first and second scenario implementation.

C. First Single Parity Bit Decoding

In the first implementation Figure 1, the probabilities of any four blocks of 2D convolved data are multiplied according to the valid sequence, considering the odd parity-check constraint. The probability of $\begin{bmatrix}1&0&0&0\\1&0&0&0\end{bmatrix}$ is found by multiplying the APP [11] for the first, APP [00] for the second, third and fourth bit. Similarly, $\begin{bmatrix}0&1&1&1\\0&1&1&1\end{bmatrix}$ of is found by multiplying the APP [00] for the first, APP [11] for second, third and fourth bit.

This continues until all the probabilities of the four-bit combination satisfying the odd parity equation are determined. There are 64 valid sequence combinations in this implementation that satisfied the odd parity check constraint for the two track ITI model. After computing the probabilities of the valid four-bit combinations, the probability of the first bits being 00 (APP [00] at the first bit position) is determined by adding the probability of sequences having 00 as first bit and dividing it with the total probabilities of all valid sequence. The same goes for 01, 10 and 11, and all the other bit positions second and third. The fourth bit position is the parity bit and is therefore ignored. This process is applied all through the data up to the end. When all tracks are processed, the parity bits are discarded and the new APPs (APP [00], APP [01], APP [10] and APP [11]) serving as the data are saved for used by across track BCJR detector for ITI cancellation.

However, in the second implementation (Figure 2), a single parity 1D MAP decoder is used across track to decode the first parity bits in the data. The output of the MAP ITI detector is passed to the decoder for decoding the parity bits. The MAP detector across track produced a soft information output which gives the APP of the detected bit being either 1 or 0. This APP is used by the decoder as data input to decode the parity bit.

4. Simulation and Implementation

4.1 Channel Simulation Model

In this paper, a two-track SMR channel with ITI of two tracks was considered. Initially, the isolated channel response *h(t)* and the jitter response (s') were evaluated using preset values of V_{max} and T_{50} .Due to ITI of the system, the jitter response is modified to include ITI by a modifying factor given as;

$$J = \sqrt{0.5\sum (s')^2 \sum (\rho)^2} \tag{13}$$

Where (s') is the jitter response of the channel and ρ represent the ITI response. $\rho = [\alpha_1, \alpha_2]$, $\alpha_1$and α_2 represent the fraction of the total amplitude read by the Read head from the two tracks.

The data is coded to contain two single parity bits based on odd parity check constrain. A sector containing 8 tracks and 4096 bits per track was assumed to hold the coded data with guard bands place between sectors. The guard band between the sectors contains -1s (zeros) written all through and the last track of a sector is assumed to be twice as wide as the preceding tracks. The latter ensures that the succeeding track is not overriding the extra width of the last track (Zheng *et al.*, 2014). Also, a portion of the first track is set to contain -1s (0s) written all through. The total noise power was set to have 80% jitter noise power and 20% additive white Gaussian noise power. The SNR in dB of the overall signal is defined by (8).

$$SNR = 10\log_{10}\left(\frac{V_p^2}{\sigma_w^2 + \sigma_j^2}\right) \tag{8}$$

where V_p is the peak voltage of the read back signal waveform. σ_j and σ_w are the standard deviations of jitter noise and AWGN respectively.

A linear equalizer of length 12 and target [0.4, 1.0,1.0, 0.4] was used for sharping the data along the track. The target length 4 ensure the detector handled the code constraint with the ITI from the side tracks serving as the target across track. The simulation model was implemented in C/C++ programming codes.

4.2 Design Evaluation

Since ITI of two tracks (k=2) and a target length of 4 are considered, our multi-level BCJR along the track will have 64 (2^{mk}) states with 4 (2^k) incoming and outgoing branches per state. However, due the single parity check constrains of the code, the number branches per state reduces to one after each three-consecutive pair of data is received.

Additionally, the fact that a portion of the first track contains -1s written all through reduces the possible states to 8 with 2 branches per state and subsequently 1 branch after every pair of three bits are received. This further reduces the complexity

of the detector and also improves performance. The same also applies to the last track.

After computing the APPs representing the probability of symbols [0, 0] up to [1, 1] across the trellis section, these values are saved for use in the ITI cancellation across tracks. The BCJR across tracks has two states with two branches entering or leaving per states. The branch metrics for the transitions are the saved APPs from the multi-level BCJR along tracks. The BCJR initially starts from one possible state with two branches, later diverges into a two-state trellis with two branches per states, and finally ends into one state. The APPs computed from the BCJR detector are then used for further processing (de-interleaving and single parity decoding as the case may be).

5. Results

The purpose of parity coding is to improve the performance of the system by detecting and possibly correcting any form of error introduced into the system. The performance of the 2D MAP joint detector decoder using the two parity coding approaches is presented in this section.

Figure 4 shows the performance of the 2D MAP joint detector decoder with parity bits along track only separated by DRP interleaver, and with parity bits in both along track and across tracks without DRP interleaver. The ITI is low (ITI [1.0. 0.25]) for data densities of $T_{50} = 1.0$ and $T_{50} = 2.0$ along track. The results show that for low ITI, the joint detector decoder with parity coding both along and across track outperformed that with parity coding along track only at both low and high ISI. A gain of round 5 dB is achieved with the former against the later coding scheme.

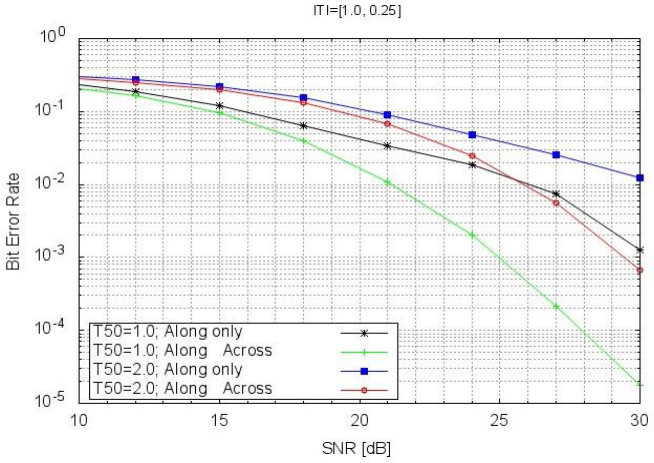

Figure 4: Comparison of parity schemes at ITI [1.0 0.25].

However, when the ITI is increased to 50% of the side track ITI [1.0 0.50] as in Figure 5, the performance coding scheme with parity bits along track only improves and closely matches that of parity bits both along track and across tracks. Still the latter outperformed the former slightly at high density ($T_{50} = 2.0$). Hence, it is not beneficial to use the both the parity bits along track only when ITI is less than 100% due additional complexity of the interleaving process.

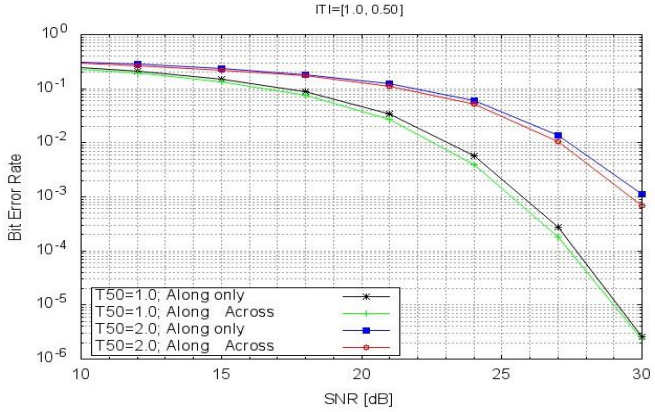

Figure 5: BER performance comparison at different T_{50}

Figure 6 shows the performance of the coding schemes when the ITI [1.0, 1.0] of the side track is increased to 100%. The coding scheme with parity bits applied along track only performed better than the scheme using parity bits along track and across tracks.

The gain achieved by the detector decoder with parities along and across track over along track only is higher, when ISI is high ($T_{50} = 2.0$) compared to low ISI ($T_{50} = 1.0$) regime as depicted by the figure. It was also observed that at high ITI and high ISI condition, the BER performance of the joint detector decoder floored at high SNR values.

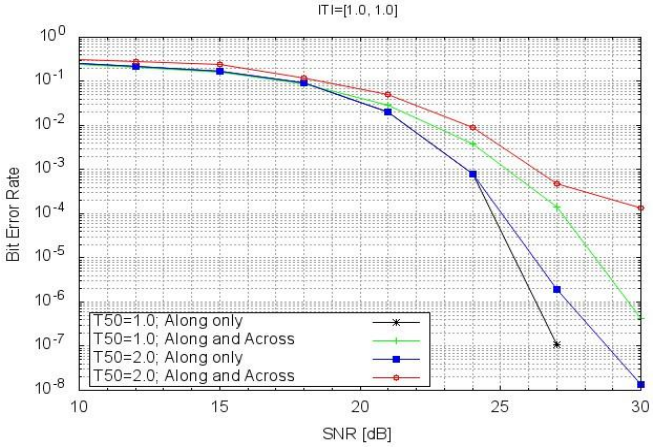

Figure 6: BER performance comparison of different ITI levels

A comparison of the performance of two coded based 2D joint detector decoder and uncoded 2D detector is shown, for various data densities, at full ITI (100% ITI of side track), in Figure 7, 8 and 9. It is seen that coded joint detector decoder with both parities along track only has the best performance. This can be attributed to the following factors. One, coding with parity check code generally improved the performance of the detector by preventing and correcting any form of error that occur in the system. This is obvious when we compare the performance of the coded system with the uncoded system.

The second factor is that for joint detector decoder with parities along track, the DRP interleaver placed in between the two parity bits provides adequate parity bit separation within the data at high data density. This randomised the noise and prevents localisation of burst errors, thereby improving the minimum distance between data and codeword. Whereas joint detector decoder with parities along track and across track, as implemented here, there is no interleaver separating the parity bits are placed in both directions.

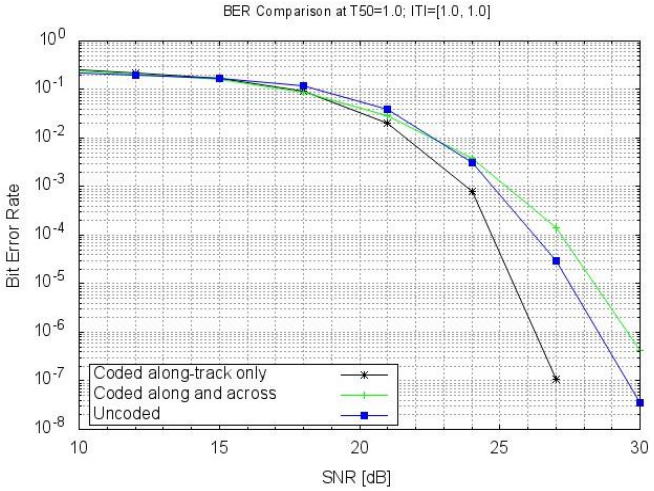

Figure 7: Performance comparison of the two coding approaches

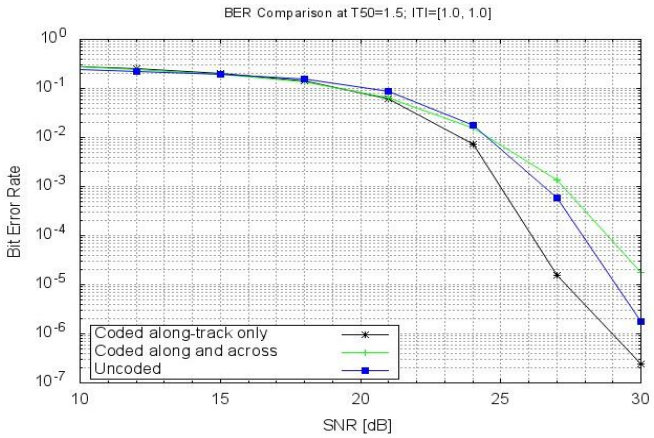

Figure 8: Performance comparison of the two coding approaches

The third factor is the fact that the 2D multi-track joint MAP detector decoder is implemented along track in both cases to start with ISI cancelation before applying the ITI detector across track. This gives an added advantage of better performances when all the parity bits are placed along track. The gain is between 2 dB to 3 dB in favour of the joint detector decoder with parities along track separated by DRP interleaver over that with parities in both along track and across tracks.

However, the gain is achieved at the expense of an additional complexity and extra latency in the system. This comes due to the interleaving, and de-interleaving processes of the DRP interleaver applied between the two parity bits along track. This increases the computational cost per symbol in the decoding process and also causes some delay processing the symbols.

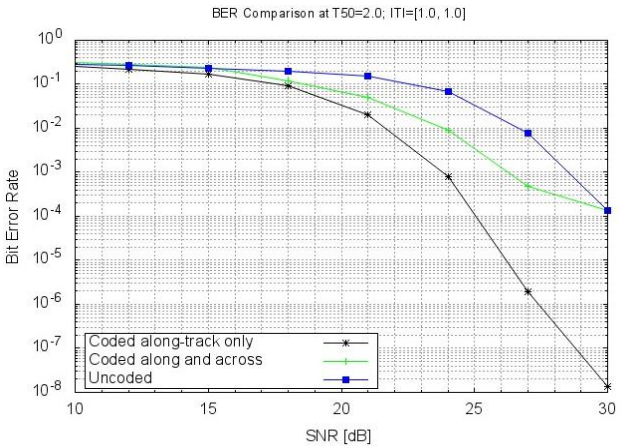

Figure 9: Performance comparison of coding approaches at different ITI levels

The summary of the comparison of the performances of the encoding schemes is given by Table 6.1. It can be therefore concluded that in general, coding with parity across and along track produce the best results in situation where there is low track density (ITI). This means that the across and along track scheme does not exploit the ITI gains. However, for channel having high track density (ITI), coding with parity bits along track only gives the best performance. The performance of the coding schemes generally decreases with increase in data density along track (T_{50}).

Table. 1. Summary of single parity coding schemes performance comparison.

	Along Track only		Along and across Tracks	
	Data density (T_{50})	Track density (ITI)	Data density (T_{50})	Track density (ITI)
LOW	Best	Worst	Best	Best
MEDIUM	Good	Good	Good	fair
HIGH	Worst	Best	Worst	worst

6. Conclusion

From the results presented here, it is shown that interchanging the direction in which the serially concatenated single parity code is applied can produce better performance in some situations; for low ITI situations, concatenating single parity codes both along track and across track directions without DRP interleaver is the best option; however, when both ITI and ISI are high it is better to use the concatenated single parity codes along track direction only separated by the DPR interleaver. As recommendation for

future works; more powerful, less complex inteleaver system other the DRP interleaver can be explored, the research can also be extended to other codes such as turbo codes and low-density parity check (LDPC) codes.

REFERENCES

Almustapha, M. D., Abdulrazaq, M. B., Ahmed, M. Z., Marcel, A. A., & Paul, D. (2016, July). Decoding and detection for magnetic recording channel using single parity coding. In *2016 Asia-Pacific Magnetic Recording Conference Digest (APMRC)* (pp. 1-2). IEEE.

Bahl, L., Cocke, J., Jelinek, F., & Raviv, J. (1974). Optimal decoding of linear codes for minimizing symbol error rate (corresp.). *IEEE Transactions on information theory*, *20*(2), 284-287.

Chan, K. S., Shafiee, S. S. B., Rachid, E. M., & Guan, Y. L. (2014, February). Optimal joint viterbi detector decoder (JVDD) over AWGN/ISI channel. In *2014 International Conference on Computing, Networking and Communications (ICNC)* (pp. 282-286). IEEE.

Chen, Y., & Srinivasa, S. G. (2013). Joint self-iterating equalization and detection for two-dimensional intersymbol-interference channels. *IEEE transactions on communications*, *61*(8), 3219-3230.

Crozier, S., & Guinand, P. (2001, October). High-performance low-memory interleaver banks for turbo-codes. In *IEEE 54th Vehicular Technology Conference. VTC Fall 2001. Proceedings (Cat. No. 01CH37211)* (Vol. 4, pp. 2394-2398). IEEE.

Guan, Y. L., Han, G., Kong, L., Chan, K. S., Cai, K., & Zheng, J. (2014). Coding and signal processing for ultra-high density magnetic recording channels. *In 2014 International Conference on Computing, Networking and Communications (ICNC)* (pp. 194-199). IEEE.

Hwang E., Negi R., and Kumar B.V..K (2010) "Signal processing for near 10 Tb/in^2 density in two dimensional magnetic recording (TDMR)", *IEEE Transaction on Magnetics* , 46(6), pp. 1831-1861

Muhammad, B. A., Mohammed, Z. A., & Paul, D. (2015, November). Concatenated 2D SOVA for two dimensional maximum likelihood detection. *In 2015 23rd Telecommunications Forum Telfor (TELFOR)* (pp. 441-444). IEEE.

N. Zheng, K. S. Venkataraman, A. Kavcic and T. Zohang, (2014). A study of multitrack joint 2-D signal detection performance and implementation cost for shingled magnetic recording. *IEEE Transaction on Magnetics*.50(6), 1-6.

Reinsel, D. Gantz, J. and Rydning, J. (2017). Data Age 2025: The Evolution of Data to Life; Don't Focus on Big Data; Focus on the Data that's Big. [*online] Framingham: IDC.*

Shafiee, S. S., Sann, C. K., & Liang, G. Y. (2015). Novel joint detection and decoding schemes for TDMR channels. *IEEE Transactions on Magnetics*, *51*(4), 1-6.

Shiroishi, Y., Fukuda, K., Tagawa, I., Iwasaki, H., Takenoiri, S., Tanaka, H., ... & Yoshikawa, N. (2009). Future options for HDD storage. *IEEE Transactions on Magnetics*, *45*(10), 3816-3822.