STUDY OF HOT-CARRIER INDUCED DEGRADATION IN DELTA-DOPED AND CONVENTIONAL MOSFETS.

ELECTRICALS

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ABSTRACT

A DC stress analysis has been performed to assess the reliability of delta-doped and conventional MOSFETs. The experimental results and 2-D computer simulations indicate that there is little variations in the threshold voltage, transconductance and drain current in the delta-MOSFET due to stress than in the conventional MOSFET.

Keywords: *Reliability, Delta-doped, Conventional, MOSFET, Subthreshold, transconductance, stress, 2-D (Two Dimensional)*

INTRODUCTION

Device reliability issues in MOSFETs have attracted much research in recent years, more especially, as device are scaled down into the sub-micron regime. Of a major concern is the hot electrons which are injected from the channel into the gate oxide [1-4]. The device characteristics degrade as more hot carries are trapped into the oxide when high fields are present. Many authors have modeled device reliability problems in terms of hot carrier ejection effects. These models have predicted the existence of hot carriers as gate currents while Hu [2] expressed it as a relation between substrate and gate currents. Others have used interface trap density as estimates of MOS reliability. It is well known that one advantage of buried channel, in general, is that the hot-carrier induced interface damage is reduced since the current flows below the interface [5], however there has not been any reported detailed study on the degradation mechanisms in δ-doped MOSFETs. In this paper, we present a study of degradation in δ-MOSFET through experiment and 2-D computer simulation.

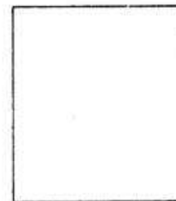
EXPERIMENTAL OBSERVATION

Conventional and delta-doped pMOSFET devices fabricated from the work of Wood *et el* [6] with dimensions (measured in microns) ranging from (W x L) ; 3 x 3 and 80 x 10 were subjected to DC stress under identical bias conditions (V_{GS} = -0.8V, V_{DS} =-4V) for a duration of 1.0 - 5.4 x 10^5 seconds. HP4155A parameter analyzer was used in the stress experiment and programmed to output the device characteristics as drain current, gate current, substrate current and transconductance after fixed intervals of stress times. The threshold voltages were determined by the TC method [7]. Figs 1(a) and 1(b) are the plots of

ΔV, ΔI and respectively against stress time in a log-log scale for the two types of devices. The plots follow the following empirical relation given by Takeda and Suzuki *et al* [4] for device degradation in terms of transconductance and threshold shifts after stress time as:

$$Y = A \times t^n \qquad (1)$$

Where A is related to the number of carriers generated by impact ionisation and n is related to the hot carrier injection mechanisms.



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The slopes of the plots (Fig. 1 (a)) of the two conventional devices are steeper than those of the delta-doped devices. Thus n is estimated to be in the range 0.23 - 0.33 for the conventional devices while for the delta-doped devices n = 0.15-0.18. Similarly from the plot of maximum transconductance versus stress time for the two types of in Fig. 1(b), the values of n are 0.13 and 0.083 corresponding to conventional and delta-doped pMOSFETs. The low value of n for the delta-doped devices implies that hot-carrier effects are relatively low in these devices in comparison with conventional devices.

SIMULATION OF HOT-CARRIER EFFECT ON 0.1μ nMOSFETs

In order to verify the experimental observation reported above and also to extrapolate into the submicron regime, two-dimensional (2-D) simulation has been performed on 0.1 μm nMOSFETs (conventional and delta-doped) using BLAZE [8]. In this study, the devices were modeled as in Roblin *et al* [9] with structural parameters identical to that reported in Diawuo *et al* [10] using an oxide thickness t_{ox} of 3.5 nm.

The effect of hot-carrier degradation on the device is modelled by introducing a sheet of fixed negative charge (2×10^{12} cm^{-2}) at the Si-SiO_2 interface near the drain end. The profile of the fixed charge distribution was Gaussian with peak value located at the drain junction and with characteristic length of 0.012 μm. An electron capture cross section, σ of 1×10^{-16} is used. The simulation was performed under bias condition of V_{GS} = 1.2V, V_{DS} = 1.0 V and stressed for 1.2×10^5 s. The position and value of the interface charge is expected to change as more charges are trapped into the Si/SiO_2 interface as the devices are stressed. The choice of the bias condition was made with the view of confining the carrier conduction in the delta-doped device to the buried channel, since the parasitic surface device is expected to turn on around V_{GS} = 1.2 V.

Figs. 2 and 3 are plots of drain current against gate voltage at fixed stress times for conventional and delta-doped nMOSFETs respectively at V_{DS} = 50 mV. The I_{DS} - V_{GS} characteristics of the conventional surface device (Fig. 2(a)) clearly shows that the threshold voltage increases with stressing while that of the delta-doped device (Fig. 3(a)) decreases with stress. The magnitude of the threshold shift in the delta-doped (= 32 mV) is lower than that of the conventional surface device (= 97 mV) for the same stress condition and duration. The conventional surface device shows a change in the subthreshold slope of approximately 4 mV/decade while that of the delta-doped device remains the same.

The I_{DS} -V_{GS} characteristics of the two types of devices are shown in Figs. 4. Note that here again the degradation in the I_{DS} -V_{GS} characteristics is less pronounced in the delta-doped devices (Fig. 4(b)) compared to that of the conventional devices (Fig. 4(a)). The degradation is quite noticeable in the linear region and in particular at the points where the drain current begins to saturate (V_{GS}- V_{th}) = V_{DS}. There is, however, less degradation in the saturation region and it virtually shows no change in the maximum transconductance (g_m) between the stressed and the unstressed devices.

ANALYSIS AND DISCUSSION ON HOT-CARRIER DEGRADATION EFFECTS IN δ-MOSFET

The comparative study of hot-carrier effects on p- and n-channel MOS devices, using experiment and simulation, presented in the previous sections shows a reduction in device degradation in the delta-doped devices. This reduced hot-carrier effect is at the moment attributed to the presence of the delta-layer within the device, but the question is how does it contribute to the reduction in hot-carrier degradation. This may be due to the reduction in the injection and trapping of carriers into the gate oxide and/or by the influence of the difference in electric field build up across the

gate. oxide when under stress or by the difference in threshold voltage in the case of the p-MOS devices (where the conventional devices are operated in enhancement mode and the delta-doped devices as depletion). In order to understand how the delta-doped devices can reduce hot-carrier induced degradation, it is worthwhile re-examining the issues related to the gate current generation.

The gate current model is based on the probability of an electron being injected into the gate oxide using the lucky electron approach based on that of Tam [1]. This can be expressed as the product of the probability P_ϕ of an

$$P_\phi = \frac{\lambda E_x}{4\phi_B}\exp\left(-\phi_B/\lambda E_x\right) \quad (2)$$

electron having sufficient momentum normal to the oxide interface to be able to surmount the oxide barrier and the probability P_{ox} of collision free travel to the $Si\text{-}SiO_2$ interface. For a

$$P_{ox} = \exp\left(-\sqrt{q/\left(16\pi E_{ox}\varepsilon_{ox}\lambda_{ox}^2\right)}\right)\frac{\int_0^{y} n(y)\exp(-y/\lambda)dy}{\int_0^{y} n(y)dy} \quad (3)$$

conventional MOSFET, P_ϕ is expressed as:

where E_x is the accelerating electric field, λ is the scattering mean free path of the hot electron and ϕ_B the $Si\text{-}SiO_2$ barrier height. P_{ox} is also expressed as:

which is the scattering probability factor exp $(-y/\lambda)$ weighted by the electron concentration in the conduction path; where λ_{ox} is the mean free path in the oxide, E_{ox} is the oxide field (in the direction from gate to substrate) and y is the distance from the $Si\text{-}SiO_2$ interface, q and ε_{ox} are the electronic charge and permittivity of silicon respectively. It can be observed in Fig. 3 (b) that stressing the delta-doped nMOSFET leads to a negative threshold shift with the resulting subthreshold characteristics identical to that of the unstressed device at a relatively higher drain bias. Thus, the introduction of negative charges at the $Si\text{-}SiO_2$ interface

$$P_{\phi\delta} = \frac{\lambda E_x}{4\phi_{B\delta}}\exp\left(-\phi_{B\delta}/\lambda E_x\right) \quad (4)$$

modifies the surface potential but can, however, be compensated by the holes in the cap layer. This will result in less charge trapping within the oxide. Therefore, for the delta-doped device, equation (2) can written as:

where $\phi_{B\delta} = \phi_B + \Delta V$, being the sum of the barrier height for the conventional device and the potential contribution due to the cap layer dose. By comparing equations (2) and (4), it is clear that the electrons have relatively higher probability of reaching the $Si\text{-}SiO_2$ interface in the conventional device than the delta-doped device.

$$P_{ox\delta} = \exp\left(-\sqrt{q/\left(16\pi E_{ox}\varepsilon_{ox}\lambda_{ox}^2\right)}\right)\frac{\int_0^{v} n(v)\exp(-(v+d)/\lambda)dv}{\int_0^{v} n(v)dv} \quad (5)$$

In addition, for the delta-doped device, the conduction carrier distribution will be further from the gate oxide by a distance d, the delta-depth. Thus the probability of collision free travel to the $Si\text{-}SiO_2$ interface P_{ox} becomes:

$$P_r = \frac{P_{ox\delta}}{P_{ox}} = \exp\left(-d/\lambda\right) \quad (6)$$

where $v = y - d$. The exact shape of the carrier distribution is likely to be slightly different in the delta-doped device, but the dominant effect on the gate oxide is the mass removal of carriers to a distance d from the oxide. This results in a relative probability reduction P_r given as

In bulk silicon, λ, the electron mean free path is around 10 nm (Tam [1]). Hence for the delta-doped device with delta-layer of 20 nm below the oxide the contribution of equation (6) to the reduction of gate current is a factor of about 7. While the electron mean free path may be different for transport along the delta-layer due to high dopant concentration, quantum and strain effects, the important mean free path as far as the gate current is concerned is the one

perpendicular to the delta-layer, which is likely to remain the same as for the bulk. It is, however, clear that the further the delta-layer is from the oxide, the lower the predicted gate current and the better the reliability of the device.

CONCLUSION

The prospects for using delta-doped buried channel nMOSFET for CMOS application has been examined by two dimensional computer simulation. It was found out that confining the conduction channel in the bulk by way of delta-doping does not improve either the performance or the short-channel effects of sub-micron MOSFET. However, there can be a remarkable improvement in the device's reliability due to a reduction of hot-carrier effects.. It has also been demonstrated that the performance of the delta-doped device can be improved by using a non-aligned gate structure to within a factor of about 85% of an equivalent conventional device.

In terms of hot-carrier induced degradation, it has been shown through experiment and simulation that the δ-MOSFET is more reliable. This is likely to be due to the fact that the conducting carriers are far removed from the oxide and in part due to the difference in the Si-SiO_2 potential barrier height.

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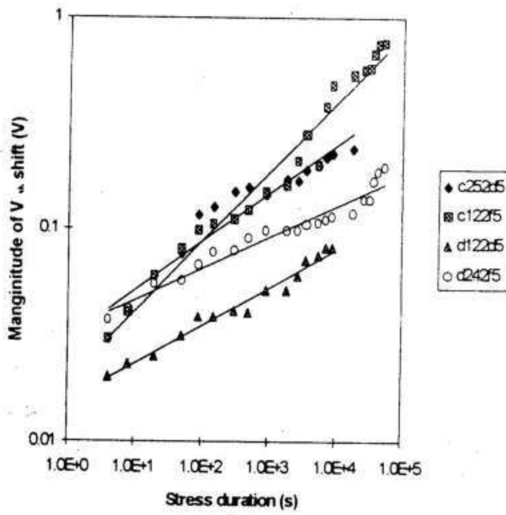

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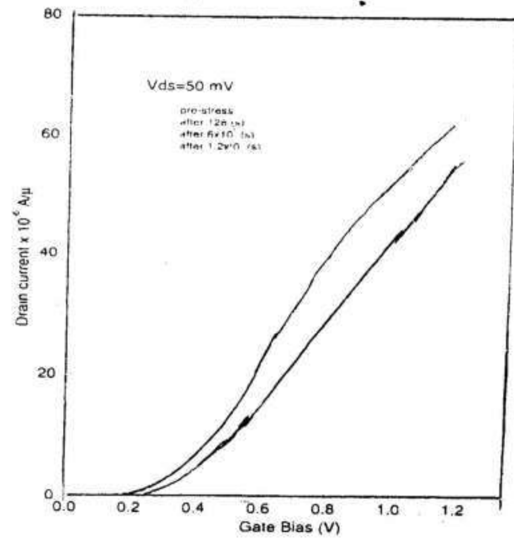

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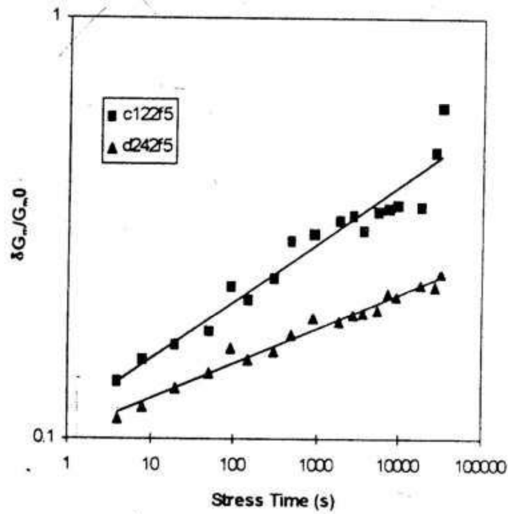

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Fig. 1 Hot-carrier induced degradation characteristics of experimental p-MOS. conventional and delta-doped devices: Leading letters c and d in device names stand for conventional and delta-doped respectively: (a) shift in threshold voltage: (b) Change in transconductance

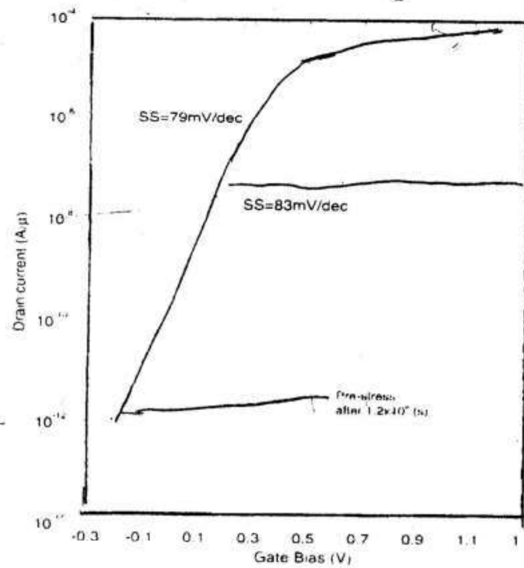

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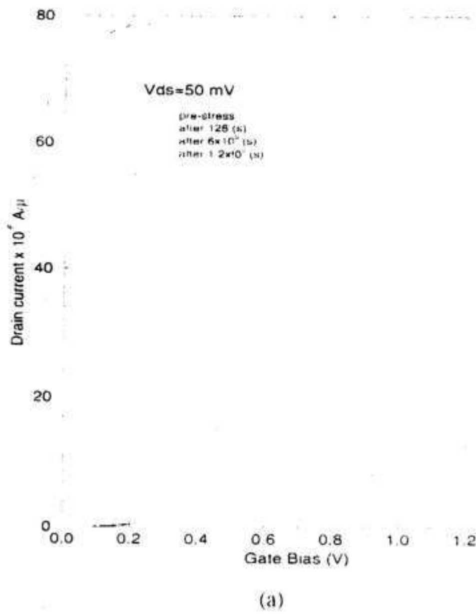
Fig 2 I-V characteristics of pre- and post-stressed conventional 0.1µm nMOSFET: (a) linear plot: (b) Sub-threshold characteristics



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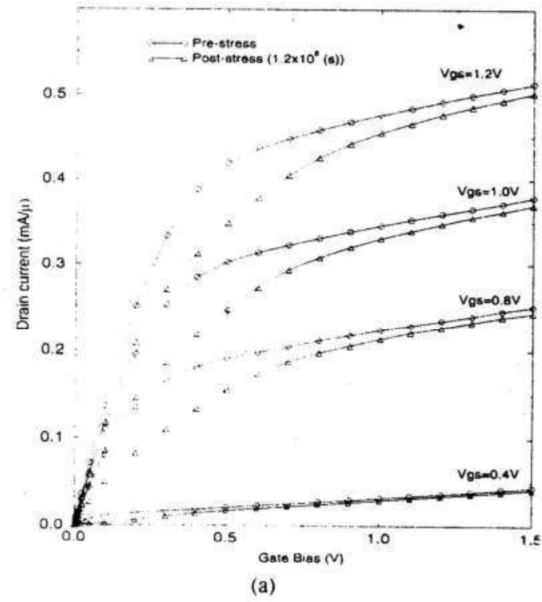

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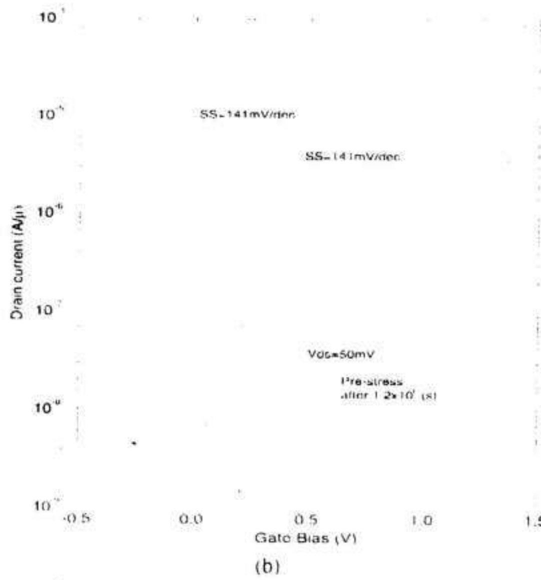

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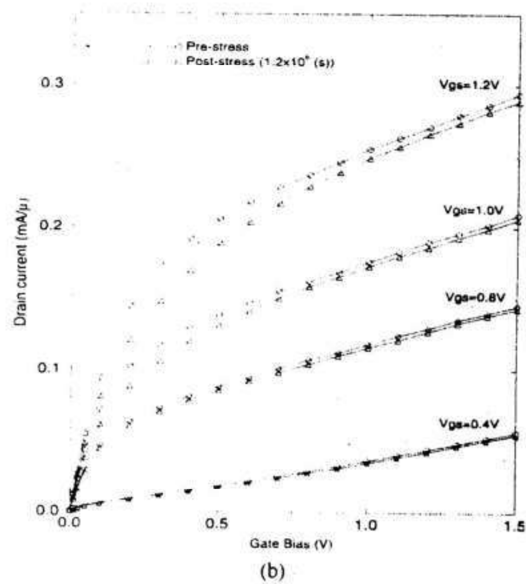

(b)

Fig 3 I-V characteristics of pre- and post-stressed delta-doped 0.1μm nMOSFET: (a) linear plot, (b) Sub-threshold characteristics

Fig 4 Complete I-V characteristics of pre- and post-stressed 0.1μm nMOSFET: (a) conventional; (b) delta-doped