COMPARATIVE STUDY OF SUB-MICRON BURIED-CHANNEL DELTA DOPED MOSFETS

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ABSTRACT

In this work, the performance of a deep-submicron δ-doped MOSFET has been evaluated in terms of its conventional counterpart using 2-D simulation. The comparison was based on the scaling law relationships reported in the literature and relative data is given for subthreshold leakage currents, DIBL, speed and cut-off frequencies. A performance figure of merit indicates the conventional device out performs that of the δ-doped MOSFET by 30%.

Keywords: *Delta-doped Buried Channel MOSFET (δ-BCMOSFET), Conventional MOSFET, Drain Induced Barrier Lowering (DIBL), subthreshold, speed, cut-off frequency.*

INTRODUCTION

The technique of delta-doping or atomic layer doping (ALD), where in the ideal case dopant atoms are distributed in a single atomic plane of the lattice host, has been used in a number of semiconductor devices since it was first proposed by Wood *et al* [1]. Their application can be found in such devices as diodes with potential barriers [2]; and δ -FET devices both in GaAs [3], [4] and in Si [5], [6] as conductive channels and as punchthrough stopper [7]. It has been proven that δ-FETs have a potential of high transconductance g_m and good high frequency f_t performance. This was demonstrated by Schubert *et al* [4] in GaAs δ-FET where an external g_m of 75 mS/mm and f_t of about 10 GHz were obtained using 0.5 μm gate length. Gorkum *et al* [5] reported of g_m value 7 mS/mm for Si δ-FET with gate length 8μm. Nakagawa *et al* [7] obtained a g_m value of 20 mS/mm for 2 μm δ-FET.

Improvements in g_m and f_t may be gained in the conventional MOSFET by scaling down the device dimensions. Hu *et al* [8], reported of device speed of 6.8 x 10^6 cm/s, subthreshold slope of 88 mV/decade and a drain-induced barrier lowing of 82 mV/V for 0.1μm nMOSFET. Similar results have also been obtained by Taur *et al* [9] with the 0.1μm nMOS device having a saturation transconductance of 620 mS/mm and f_t of 118 GHz. These high performance devices have been achieved through advancement in technology and vigorous scaling methods. Scaling down MOFETs improves the speed, however, the performance can be degraded by other related issues as short-channel effects, choice of power supply versus threshold voltage, subthreshold current and hot-carrier reliability. It is expected that by removing the hot-carriers from the Si/SiO_2 interface may reduce the interface scattering and increase the device speed in submicron MOSFET's in the same way as using heterojunction channels.

Delta-doped buried channel MOSFETs (δ-BCMOSFET's) are therefore expected to have the potential to suppress short-channel effects as devices dimensions become smaller [5], [7]. This paper presents a comparative study of a buried delta-doped channel MOSFET for submicron CMOS application using 2-D simulation. By focusing on n-channel device, the performance is reported and examined relative to that of conventional 0.1μ MOSFET reported in Hu *et al* [8] and O'Neill *et al* [10].

DEVICE SIMULATION

The basic structure of delta-doped buried channel nMOSFETs used in the study is shown in Figure 1. Some requirements imposed on the δ-nBCMOSFET, if it is to be used in CMOS applications are that the device be enhancement mode, ideally without substrate biasing, that the device can switch within a useful voltage range without surface conduction channel turning on, and that leakage current be acceptably low.

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The delta-doped buried channel device (Figure 1) consists of bulk substrate doping of 4.2 x 10^{17} cm^{-3}, source/drain dopant concentration of 10^{20} cm^{-3}, and abrupt 40nm source/drain junction, and gate oxide of 5nm as reported by Diawuo *et al* [11]. The delta-layer is defined between two spacer layers of doping concentration $10^{15}cm^{-3}$ each with thickness of 10 nm.

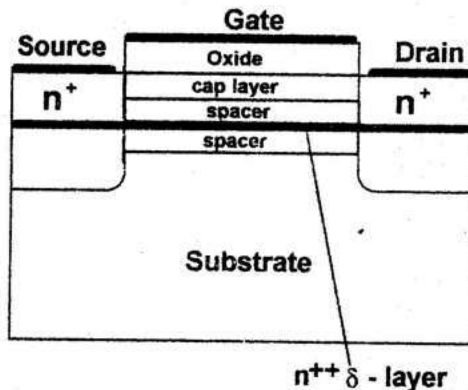

Figure 1: Schematic representation of Delta-Doped Buried Channel MOSFET Structure used in this work.

The delta-layer has a Gaussian profile with standard deviation of 3.5 x 10^{-4} μm and peak concentration of 7.5 x $10^{19}cm^{-3}$ occurring at a depth 19 nm below the interface. Just below the interface a cap layer of 10 nm thick with a doping concentration of 7.5 x $10^{18}cm^{-3}$ has been introduced to act as an initial potential barrier to surface conduction.

The conventional nMOSFET used as a monitor to the delta-doped buried channel device has doping profiles as that used in the simulations undertaken by Hu *et al* [8]. The nMOSFET has a uniform substrate doping of 1 x $10^{17}cm^{-3}$, source/drain doping of 10^{20} cm^{-3}; an abrupt 30 nm source and drain junctions; n^+- polysilicon gate material and gate oxide of 5 nm. Threshold voltage implant was used to adjust the device's threshold voltage to be between 0.2V and 0.3V to be the same as that of the δ-nBCMOSFET. In the simulation, these values are taken as default structural parameters throughout the investigation unless otherwise stated.

PHYSICAL MODELS AND NUMERICAL METHODS

A 2D simulator, BLAZE [10] is used to simulate both conventional and δ-nBCMOSFET with channel lengths ranging from 0.5 μm down to 0.1 μm and gate oxide thickness from 3.5 nm to 10nm. The hydrodynamic energy balance model is employed which includes non-local carrier heating effects and provides a self-consistent solution of the drift diffusion and energy balance equations. This model is recommended for simulating submicron device but is computationally expensive. To speed up the simulation process the drift diffusion model is used to evaluate the threshold voltages. The drift diffusion, due to its remarkable efficiency and speed is preferred to both Monte Carlo method and energy balance model when evaluating I-V characteristics under bias conditions for which no relevant hot-carrier effects occur. This model is initially used to determine the default parameters of the delta-doped device through a number of simulations.

The hydrodynamic model is then used to evaluate all the other device parameters involving bias voltages greater than the threshold voltages. In adopting this model, the carrier mobility's and impact ionisation coefficients are allowed to be functions of carrier temperature. The carrier temperature dependent mobility used is that reported in BLAZE [12] and requires the homogeneous energy balance equation to be consistent with the field dependent mobility model. In particular for the δ-nBCMOSFET, only the conduction in the buried channel is of interest in this study, therefore the parallel field mobility is the most appropriate. Thus

$$q\mu_n(E_{eff})E_{eff}^2 = \frac{3}{2}k\frac{T_n - T_L}{\tau_{en}} \qquad (1)$$

where T_n is the carrier temperature, T_L is the lattice equilibrium temperature, τ_{en} is the energy relaxation time, and the mobility, μ_n is a function of the parallel electric field E_{eff} as given by Caughey and Thomas [13]

$$\mu_n(E) = \left[\frac{1}{1 + \left(\frac{\mu_o E}{V_{sat}} \right)^{\beta}} \right]^{\frac{1}{\beta}} \mu_{on} \tag{2}$$

where β is a constant equal to 2 for elections (similar relationship holds for holes with $\beta = 1$); and $V_{sat} = 1.03 \times 10^7$ cm/s is the saturation velocity. The low field mobility μ_{0n} which is also temperature dependent is that given by Caughey and Thomas [13] and Selberherr [13] for electrons as:

$$\mu_{0n} = \mu_{1n} \left[\frac{T}{300K} \right]^{\alpha n} + \frac{\mu_{2n} \cdot \left[\frac{T}{300K} \right]^{\beta_n} - \mu_{1n} \cdot \left[\frac{T}{300K} \right]^{\alpha_n}}{1 + \left[\frac{T}{300K} \right]^{\gamma_n} \cdot \left[\frac{N}{N_{cn}} \right]^{\delta_n}} \tag{3}$$

where N is the local (total) impurity concentration in cm^{-3} and T is the temperature in degree Kelvin. Non default parameters for silicon at T_L = 300K are μ_{ln} and μ_{2n}. These values of μ_{ln} are chosen to ensure consistent results with those of O'Neill *et al* [10]. The value of μ_{2n} is taken as 1245cm^2/Vs for all regions of the device. For the conventional device μ_{ln} is taken as 425cm^2/Vs while for the delta-doped buried channel device, μ_{ln} in the delta-layer is 90cm^2/Vs, 750 cm^2/Vs for the spacer regions and 110cm^2/Vs for the cap layer.

METHOD OF ANALYSIS

Hu *et al* examined the basic MOSFET scaling laws in relation to performance by expressing the variables channel length, the drain-induced barrier lowering (*DIBL*) and *speed* (g_m/WC_{ox}) in power form. The power law relationships among the three fundamental device variables are:

$$L_c = \Theta(DIBL)^{\theta} \tag{4}$$

$$Speed = \Lambda(L_c)^{\lambda} \tag{5}$$

$$Speed = \Gamma(DIBL)^{\gamma} \tag{6}$$

where *DIBL* is expressed as:

$$\frac{\delta V_t}{\delta V_{DS}} = \frac{V_t|_{V_{DS} = 0.05V} - V_t|_{V_{DS} = 1.5V}}{1.45} \tag{7}$$

where V_t is defined as the gate voltage, V_{GS}, corresponding to drain current,

$$I_{DS} = 10^{-7} \frac{W}{L_c} A$$

at source-drain voltage, V_{DS} of 50 mV, with W and L_c the device width and length respectively; *speed* is defined as g_m/WC_{gc}; g_m is the maximum saturated transconductance at a particular drain bias; C_{gc} is the gate to channel capacitance per unit area. $\Theta, \Lambda, \Gamma, \beta, \lambda$ and γ are constants dependent on the device's structural parameters. These constants are determined from the results of a set of experiments/simulations of MOS devices with channel lengths L_c varying from 0.5 μm down to 0.1 μm and gate oxide varying from 3.3 nm to 10.3 nm using non-linear regression of the form:

$$log(Y_i) = A + B. log(X_i) \tag{8}$$

where i is the number of samples and X_i and Y_i are the samples of L_c, *DIBL* and *speed*. The constants A and B correspond to the proportionality constant and power coefficient in equations (4) – (6). The cut-off frequency f_t, is an important parameter in characterising the performance of sub-micron MOS device as demonstrated in the work of O'Neill *et al* [10].The cut-off frequency f_t is calculated from the expression:

$$f_t = \frac{g_m}{2 \pi C_{gc}} \tag{9}$$

where g_m is the drain transconductance and C_{gc} is the gate to channel capacitance. For the delta doped buried channel devices, this capacitance is given by:

$$C_{gc} \approx \frac{C_{ox} C_s}{C_{ox} + C_s} \tag{10}$$

where C_{ox} is the gate oxide capacitance and C_s is the capacitance due to the depletion layer between gate and the buried channel. Both g_m and C_{gc} are calculated from the simulated device at a given gate and drain voltages.

RESULTS AND DISCUSSION

The plot of the drain current against gate bias of the simulated conventional and buried delta –

doped devices with 0.1 μm channel length and gate oxide thickness of 5nm are shown in Figures 2a and 2b. The two devices have the same threshold voltage of approximately 0.25V and show good switching characteristics. The subthreshold slopes and the *DIBL* extracted are 137 mV/decade and 334.4 mV/V for the delta-doped device and 95 mV/decade and 156 mV/V for the conventional device. The calculated *speeds* and f_t for the delta-doped and the conventional devices are: 4.65 x 10^6 cm/s 74.3 GHz; and 7.09 x 10^6 cm/s and 129 GHz respectively. The respective drain transconductance g_m, are 215 mS/mm and 548 mS/mm measured at bias conditions of $V_{ds} = V_{gs} = 1.0$V. The *speed* and *ft* values for the δ-nBCMOSFET are both low compared with those of the conventional device. The subthreshold slope of the δ-nBCMOSFET is not as steep as the slope of its conventional counterpart and also shows relatively high subthreshold currents.

The $I_{DS} - V_{DS}$ characteristics of the two types of devices for different V_{GS} are shown in Figure 3a and 3b. From the plots, it is quite evident that the delta-doped device shows more short channel effects than its conventional counterpart as the current saturation characteristics are better in the conventional device. The drain current is lower in the delta-doped device for a given gate bias which gives the indication that the carrier conduction is higher in conventional devices compared to that of the delta-doped device. The issue of carrier conductivity is further emphasised by examining the point along the conduction channel for which velocity overshoot occurs. The average electron velocity V_x along planes in the conduction channel can be evaluated from the expression as in O'Neill *et al* [10]

$$v_x = \frac{I_{ds}}{q\int n_x dy} for 0 \le x \le L_c \qquad (11)$$

Where I_{ds} is the channel current, n is the electron charge density, q is the electronic charge, and L_c is the channel length.

The electron charge density is calculated by integrating along the depth of the planes perpendicular to the direction of I_{ds}. The results

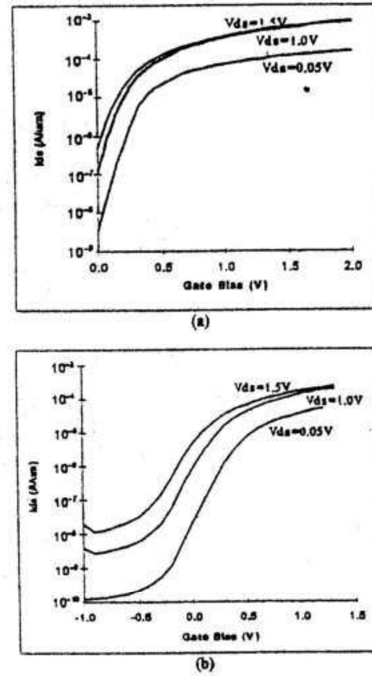

Figure 2: Drain-current versus gate-source voltage characteristics of 0.1 μm nMOSFETs with t_{ax} = 5nm. (a) conventional device and (b) delta-doped buried channel device.

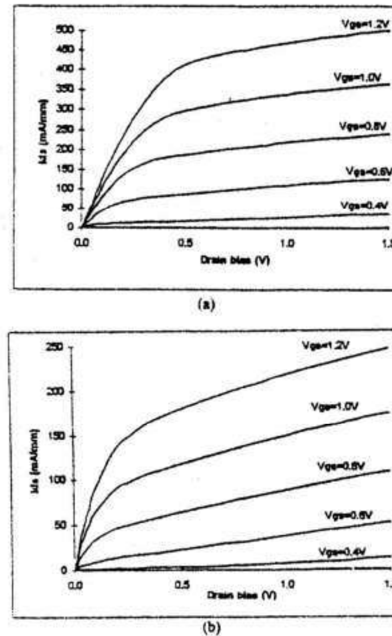

Figure 3: Drain-current versus drain-source voltage characteristics of 0.1 μm nMOSFETs with t_{ox} = 5 nm. (a) conventional device and (b) device and (b) delta –doped buried channel device.

show good agreement between the present simulation for the 0.1μm conventional nMOSFET and that undertaken by O'Neill *et al* [10] under identical bias conditions of $V_{gs} = V_{ds} = 1.0V$. In the simulation presented here the relaxation time is assumed to be dependent on carrier temperature in the hydrodynamic model.

Figure 4 shows the electron velocity profiles of 0.1μm delta-doped buried channel and conventional nMOS devices. From the figure, it can be observed that the carriers have velocities in excess of V_{sat} (1.03×10^7cm/s) beyond 40 nm from the source in the case of the conventional device, consistent with that reported by O'Neill *et al* [10], while this point occurs at 56 nm in the case of the delta-doped device. Thus from this analysis it can be inferred that the impact of velocity overshoot is less significant for the δ-nBCMOSFET as it happens close to the drain.

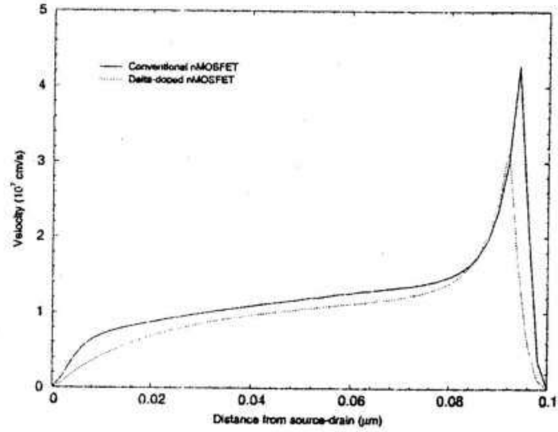

Figure 4: Plot of Velocity profile along the channel of 0.1 μm nMOSFETs with $t_{ox} = 5$ nm: conventional device (solid line), delta-doped buried channel (dotted line)

The calculated f_t is plotted as a function of channel length for both conventional and delta-doped nBCMOSFETs in Figure 5. Also shown on the plot are some experimental f_t values for conventional MOSFETs taken from the literature [9],[14]-[16]. There is good agreement between the results which increases confidence in the simulated results. For the channel lengths considered, the f_t of the delta-doped nMOSFETs are about 40-45% lower than those of the conventional devices.

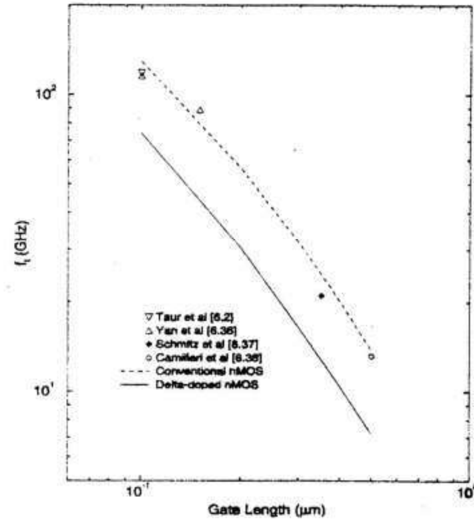

Figure 5: f_t versus channel length ranging from 0.1μm to 0.5μm for nMOSFETs with t_{ax} = 5nm: conventional (dashed line) and delta-doped buried channel (solid line). Good agreement is obtained between this simulation and experimental data taken from the literature for conventional MOSFETs.

Simulations have been performed for δ-nBCMOSFETs with channel drawn lengths ranging from 0.1μm to 0.5μm and oxide thickness ranging from 3.5 to 10 nm. Devices within similar range of gate lengths reported in Hu *et al* [8] are considered and evaluated using the power laws with confidence factor *r*, given as:

$$r = \frac{n\left(\sum X_i Y_i\right) - \left(\sum Y_i\right)}{\left\{n\sum X_i^2 - \left(\sum X_i\right)^2\right\}\left[n\sum Y_i^2 - \left(\sum Y_i\right)^2\right]^{\frac{1}{2}}} \quad (12)$$

where X_i and Y_i are the sample variables de previously. Figure 6 shows the variation of *speed* (g_{m}/WC_{gc}) with gate lengths ranging from 0.1μm to 0.5μm delta-doped nMOSFETs with t_{ox} of between 3.5 nm and 10 nm; also shown is that of a conventional 0.1μm nMOSFET with t_{ox} of 5 nm.

Here again, the g_m/WC_{gc} values of the conventional device are higher than those of the delta-doped devices. For the delta-doped nMOSFETs, with the same doping profile and source/drain geometry, the speed and channel length relationship show the same trend as that of the conventional devices for decreasing t_{ox}. This trend has been attributed to low carrier mobility resulting from high fields as the gate oxide is reduced. Thus λ is equal to 0.45 and r is –0.998 for the delta-doped devices. The plot of the channel drawn length against *DIBL* is shown in Figure 7, and again the power law relation holds for both conventional and delta-doped devices. It can be noticed on this plot that the delta-doped devices show higher values of *DIBL* compared to the conventional counterpart. However, the values of Θ (=0.45) and r (=-0.998) are the same in both types of devices. The high value of the *DIBL* in the delta-doped devices is reported in Hu and Bruce [17] as being typical of buried channel devices as they are more susceptible to punch through than the conventional device. This is thought to be due to the fact that the conducting channel is farther away from the oxide-silicon interface leading to lesser gate control over the channel.

To verify the universal trade-off relationship between performance and short-channel effects, the simulated speed (g_m/WC_{gc}) and *DIBL* are plotted in Figure 8. Conventional nMOS devices with t_{ox} of 5 nm are plotted alongside those of the delta-doped devices for comparison. The same power coefficient of $\gamma = 0.20$ is obtained for the two types of devices while the proportionality coefficient Γ are 0.15 – 0.16 and 0.40 for the delta-doped and conventional devices respectively with an average r-value of θ.995. The universal trade-off relationship between g_m/WC_{gc} and *DIBL* for conventional devices also holds for delta-doped devices since the plots of δ -doped MOSFETs with channel lengths ranging from 0.5μm down to 0.1μm and t_{ox} of between 3.5 nm to 10 nm lie almost on a straight line. The trade-off relationship between g_m/WC_{gc} and *DIBL* as indicated on Figure 8, appears to hold for devices with the same type of channel configuration and structural parameters since those of the delta-devices do not fall on the same curve as that of the conventional device.

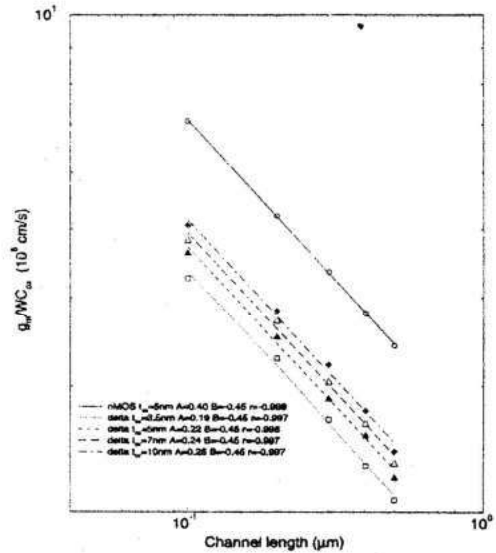

Fig 6: Simulated device speed (g_m/WC_{ox}) versus channel length for delta-doped buried channel nMOSFETs with t_{ox} = 3.5, 5, 7, 10 nm. Also shown (solid line) is that of a conventional nMOSFET with t_{ox} = 5 nm

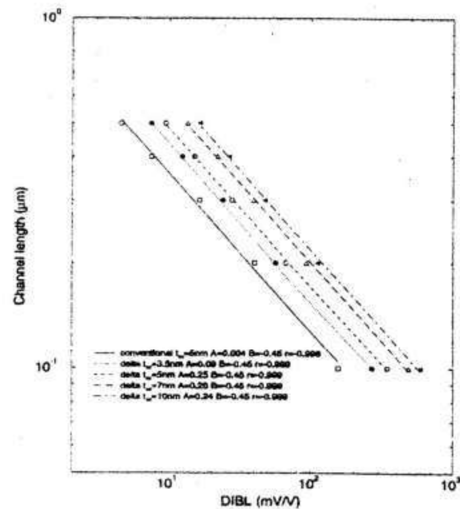

Figure 7: Plot of channel length versus drain-induced barrier lowering, *DIBL* for delta-doped buried nMOSFETs with t_{ox} = 3.5, 5, 7, 10 nm. Also shown (solid line) is that of a conventional nMOSFET with t_{ox} = 5 nm

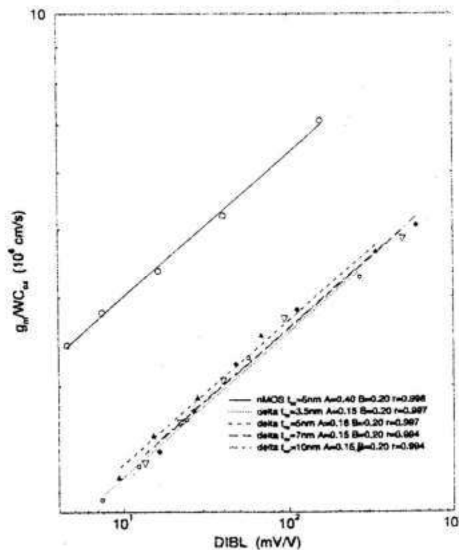

Figure 8: Simulated device speed (g_m/WC_{ox}) versus drain-induced barrier lowering, *DIBL* for delta-doped buried channel nMOSFETs with t_{ox} = 3.5, 5, 7, 10 nm. Also shown (solid line) is that of a conventional nMOSFET with t_{ox} = 5 nm

By comparing the relative positions of the *speed* versus *DIBL* plot for the two types of devices it becomes quite obvious that the conventional devices show better performance than the delta-doped devices. A similar result is reported in the work of O'Neill *et al* [9] by plotting the "universal" curves for SiGe HNMOS devices and the conventional MOSFET devices which re-enforces the notion that the trade-off relationship between *speed* and *DIBL* is only universal for a particular type of channel configuration such as heterojunction, delta-doped or conventional.

In order to quantify the performance of the delta-doped device in relation to the conventional device, we adopt a performance factor defined as:

$$P_f = \frac{\log(speed)_\delta / \log(DIBL)_\delta}{\log(speed)_c / \log(DIBL)_c} \times 100\% \qquad (13)$$

where the subscripts δ and c stand for delta-doped and conventional devices respectively. From the simulated results of 0.1μm nMOSFET, we obtain for the delta-doped device, a performance factor of 73%.

CONCLUSION

The prospects for using delta-doped buried channel nMOSFET for CMOS application has been examined by two-dimensional computer simulation. It was found that confining the conduction channel into the bulk by way of delta-doping does not improve either the performance or the short-channel effects of sub-micron nMOSFET. Simulated f_t was about 40% lower than the conventional device and *DIBL* was higher in the delta-doped device. In addition current drive capability was also found to be lower in the δ-BCMOSFETs. It was also demonstrated that the concept of universality between *speed* (g_m/Wc_{ox}) and *DIBL* relationship as reported in Hu *et al* [8] only holds for the same types of channel configuration and material properties.

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