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BACKSTEPPING CONTROL OF THREE-PHASE THREE-LEVEL FOUR-LEG SHUNT ACTIVE POWER FILTER

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ABSTRACT

In this paper, backstepping control for three-level four-leg shunt active power filter (SAPF) system is proposed. The adopted filtering topology requires both a three-dimensional space vector modulation (3DSVM) for controlling the three-level four-leg inverter as well as DC voltage and filter currents control. The regulation of the DC voltage and filter currents is accomplished by backstepping controllers. The voltage-balancing control of two split DC capacitors of the three-level four-leg SAPF is achieved using three-level three-dimensional space vector modulation equipped by a balancing strategy based on the effective use of the redundant switching states of the inverter voltage vectors. The simulation results show the effectiveness of the proposed filtering system in terms of the compensation of the harmonics and the zero sequence current and the operation at unity power factor.

Keywords: shunt active power filter; three-dimensional space vector modulation; multilevel four-leg inverter; backstepping control; synchronous reference frame theory.

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1. INTRODUCTION

Three-phase four-wire distribution power systems are widely used in office buildings, commercial complexes, manufacturing facilities and so on, to supply lower-level voltage. The loads connected to the three-phase four-wire distribution power system may be either single-phase or three-phase loads. The typical loads connected to the three-phase four-wire distribution power system may be computer-related facilities, office automatic machines, adjustable speed drives, lighting ballasts and other power electronic-related facilities. Most of these loads have the nonlinear input characteristic, which creates the problems of high input current harmonic distortion, and load unbalance. The third harmonic is most serious in the single-phase nonlinear loads. The neutral conductor is the current path of zero-sequence current. Thus, the three-phase four-wire distribution power systems have the problems of harmonic pollution and overloading of the neutral conductor [1-2].

Conventionally, the passive power equipment is used to solve the problems of the three-phase four-wire distribution power system. Passive power filters were conventionally used to solve the harmonic distortion problems. However, they have the following disadvantages [3-5]:

1- The filtering characteristics are seriously affected by system impedance.
2- A parallel resonance between the load and a passive power filter causes the amplification of harmonic currents on the source side at specific frequencies.
3- A passive filter may fall into the series resonance with a voltage source so that the voltage distortion produces excessive harmonic currents flowing into the passive filter.
4- The tuned frequency cannot vary under the different harmonic load currents.

Shunt active power filters have attracted considerable attention as an efficient way to perform power conditioning tasks such as harmonic elimination, reactive power compensation, load balancing, and neutral current elimination [7-8]. In addition, SAPFs offer high efficiency [6] and perform effectively on lower-order harmonics such as 3rd, 5th, 7th which are generated by the nonlinear loads [7].

Four-wire SAPFs has been presented in three-phase four-wire systems under three main

typologies [8-13] namely, split-capacitor or (capacitor midpoint), three single-phase bridge configuration or (H-bridge), and four-leg topology.

In the first topology, the neutral wire is connected to the midpoint of the DC-link capacitors; this topology suffers from problems such as capacitor voltage unbalance, requirement of expensive and large value of capacitors in case of large neutral current, and inefficient DC-bus utilization [13]. In the second topology, three single-phase full bridge voltage source inverters are used to realize the four-wire SAPF [13]. These H-bridge inverters are connected to the three-phase four-wire system by using three single-phase isolation transformers. Since this topology requires a transformer, the four-wire SAPF size is large and the system cost is high. Slow response and increased number of switching devices are the other disadvantages of this topology [13]. In the third topology the neutral wire is connected to the additional fourth leg, this topology has been shown to be a solution for inverters operating in three-phase four-wire systems and it offers full utilization of the DC-link voltage and lower stress on the DC-link capacitors [13].

On the other hand, most SAPFs are based on the standard two-level voltage source inverters. These compensators have limitations in medium and high voltage application due to semiconductor rating constraint. Generally, high power transformer is required for interfacing the two-level SAPF to the power system which causes more losses and high cost of installation.

In order to improve the compensation characteristics of the SAPF, multilevel inverters have been successfully introduced [14-17]. Multilevel topologies are effective in high voltage applications as they provide high output voltages with same voltage rating of individual device and eliminates the need of transformers [19-22]. In addition, they are able to generate output voltages and currents with low harmonic distortion as well as to reduce voltage stress across switching devices.

The performances of the SAPF depend strongly on the modulation technique used. Among the existed pulse-width modulation (PWM) techniques, the space vector modulation (SVM) stands out because it offers significant flexibility to optimize switching waveforms and it is well suited for digital implementation [23]. In the four-leg inverter, as the sum of

the three-phase voltage is not equal to zero, a three-dimensional SVM (3DSVM) must be adopted. Currently, the conventional 3DSVM algorithm is mainly based on the abc coordinate system [24-25] or αβo coordinate system [26-27].

Unfortunately, the SAPF built based on the multilevel inverter has an inherent problem of DC-link capacitors voltages variations. To avoid this problem several approaches have been suggested to balance the DC capacitor voltages of multilevel inverters. Some methods are based on the idea of adding auxiliary power circuits in order to redistribute the electrical charge between capacitors [28]. A very interesting solution proposed in [29], is to use the 3DSVM to stabilize the capacitors voltages in three-level four-leg inverter. The idea is to minimize a cost function defined as the quadratic sum of the differences between the capacitors voltages and their reference values [29]. Thanks to an appropriate selection of the redundant vectors this function can be minimized to zero and the capacitors voltages will be kept at their reference values [29].

It is well established that conventional linear PI controllers are widely used in most industrial power electronics applications for the reasons of their simplicity and feasibility [30]. On the other hand, it is a fact that such kinds of controllers may fail to meet the high performance requirements of grid connected inverter applications due to their high vulnerability to the operation point, variations of the plant parameters and external disturbances. In order to improve the performance of three-phase shunt active power filter, various nonlinear control strategies have been reported in the literature. The proposed control strategies include among others sliding mode control [31], passivity control [32], fuzzy control [33-34], neuron-fuzzy control [35], Lyapunov theory [36], and robust control [37].

In this work, a nonlinear control strategy based on backstepping is applied to the control of a three-level four-leg SAPF. The backstepping method will be used for developing the currents and DC voltage controllers. The capacitor voltages stability is guaranteed using three-level 3DSVM. The proposed four-leg SAPF is suitable for harmonic current reduction, reactive power compensation and neutral current elimination in a three-phase four-wire power system.

This paper is organized as follows. In section 2, the configuration of four-leg SAPF is presented and the system model is developed. In section 3, the backstepping control of the

three-level four-leg SAPF is investigated. The backstepping controllers are synthesized and the synchronous reference frame theory is presented also in this section. Three-level 3DSVM with balancing capability is performed in section 4. In section 5, the performances of controlled system are verified by simulation results. Finally, in section 6 some conclusions are established.

2. FOUR-LEG SAPF CONFIGURATION

Fig. 1 presents the shunt active filter topology based on a three-phase four-leg voltage source inverter; the four-leg SAPF is connected in parallel with the AC three-phase four-wire system through three inductors. The capacitors are used to store energy and the inductances are used to smooth and decrease the ripples of the harmonic currents injected by SAPF. Three single-phase diode rectifiers as non-linear loads are connected to the power system, in order to produce an unbalance, harmonic and reactive current in the phase currents and zero-sequence harmonics in the neutral current.

The main task of the proposed SAPF is to reduce harmonic currents, to ensure reactive power compensation and to suppress the neutral current from the source through the fourth leg of the inverter.

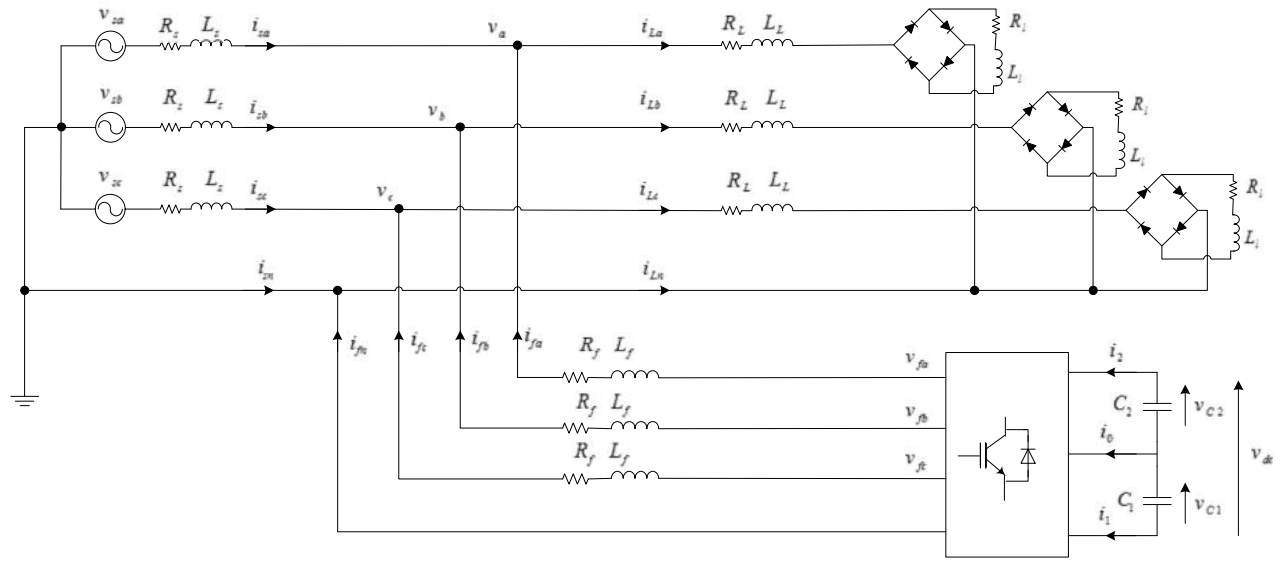


Fig.1. Structure of three-level four-leg SAPF

2.1 Mathematical model of three-level four-leg SAPF

The topology of the three-level four-leg inverter is shown in Fig. 2. Here, v_x and i_{fx} , $x = a, b, c,$ represent the point of common coupling (PCC) voltages and AC side currents of the SAPF, respectively. R_f is a line resistance that models the parasitic resistive effects of the inductor L_f. The capacitances of input capacitors are assume equal C_1=C_2=C. For a net DC-side voltage of v_{dc}, each capacitor voltage is ideally $v_{Cj} = v_{dc}/2$, $j = 1, 2$.

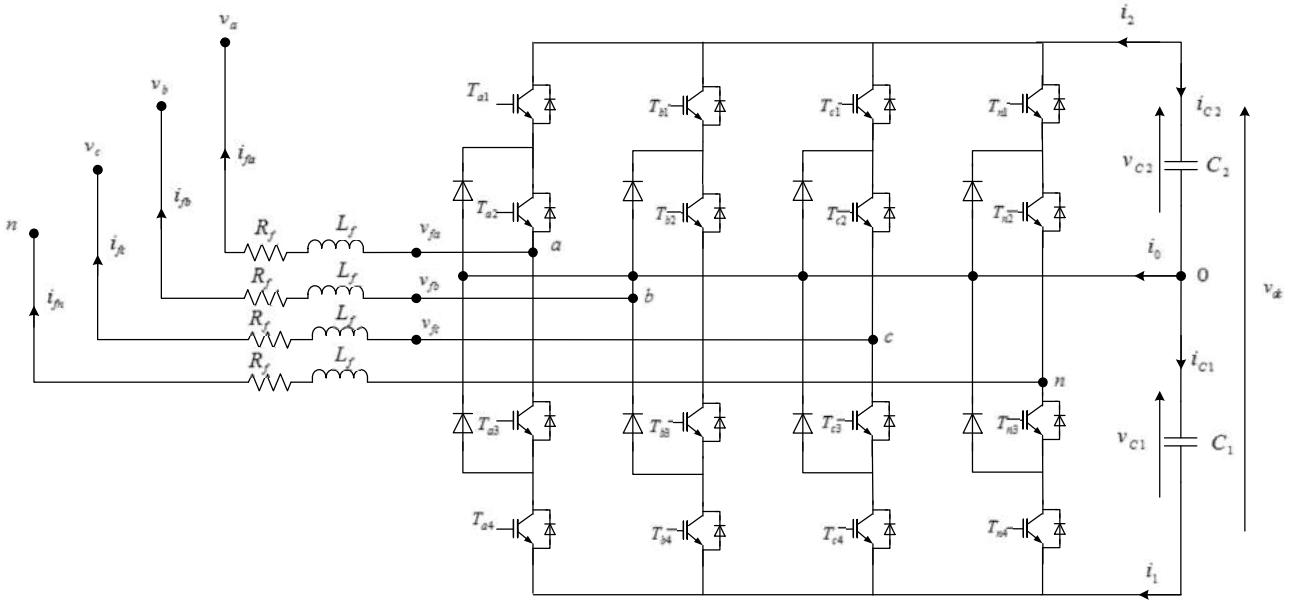


Fig.2. Schematic representation of three-level four-leg inverter

The switching functions are defined as F_{ij} where $i \in \{a,b,c,n\}$ is the phase and $j \in \{0,1,2\}$ is the voltage level. F_{ij} takes value "1" if *i*-phase is connected to voltage level *j* and "0" otherwise; these switching functions can be expressed as:

$$\begin{aligned} F_{x2} &= T_{x2}\ T_{x1} \\ F_{x1} &= T_{x2}\ T_{x3} \qquad x = a,b,c \text{ or } n \\ F_{x0} &= T_{x3}\ T_{x4} \end{aligned} \tag{1}$$

The instantaneous AC inverter phase to neutral voltages v_{fa}, v_{fb} and v_{fc} can be expressed in terms of switching functions and DC capacitor voltages as given by:

$$\begin{bmatrix} v_{fa} \\ v_{fb} \\ v_{fc} \end{bmatrix} = \begin{bmatrix} F_{a2}-F_{n2} & F_{a1}-F_{n1} & F_{a0}-F_{n0} \\ F_{b2}-F_{n2} & F_{b1}-F_{n1} & F_{c0}-F_{n0} \\ F_{c2}-F_{n2} & F_{c1}-F_{n1} & F_{c0}-F_{n0} \end{bmatrix} \begin{bmatrix} v_{C2}+v_{C1} \\ v_{C1} \\ 0 \end{bmatrix} \tag{2}$$

The mathematical equations which govern the behaviour of the AC-side of SAPF are:

$$\begin{aligned} \frac{di_{fa}}{dt} &= \frac{1}{L_f}(v_{fa} - v_a - R_f\, i_{fa}) \\ \frac{di_{fb}}{dt} &= \frac{1}{L_f}(v_{fb} - v_b - R_f\, i_{fb}) \\ \frac{di_{fc}}{dt} &= \frac{1}{L_f}(v_{fc} - v_c - R_f\, i_{fc}) \end{aligned} \tag{3}$$

The DC side of the SAPF can be expressed as:

$$\frac{dv_{dc}}{dt} = \frac{i_1 - i_2}{C} \tag{4}$$

i_1 and i_2 are the DC-side intermediate branch currents.

The DC side dynamic equation can be written as follows:

$$\frac{dv_{dc}}{dt} = \frac{i_{dc}}{C_{eq}} \tag{5}$$

Where: i_{dc} is the equivalent capacitor current, $i_{dc} = i_1 - i_2$ and C_{eq}=C/2 is the equivalent capacitance.

Based on the Concordia coordinates transformation, the differential equations describing the dynamic model of the four-leg SAPF in ~ o reference frame are given by (6):

$$\begin{aligned}
\frac{di_{f\sim}}{dt} &= \frac{1}{L_f}(v_{f\sim} - v_{\sim} - R_f i_{f\sim}) \\
\frac{di_{f}}{dt} &= \frac{1}{L_f}(v_{f} - v - R_f i_{f}) \\
\frac{di_{fo}}{dt} &= \frac{1}{L_f}(v_{fo} - v_{o} - R_f i_{fo}) \\
\frac{dv_{dc}}{dt} &= \frac{i_{dc}}{C_{eq}}
\end{aligned} \tag{6}$$

3. BACKSTEPPING CONTROL OF THREE-LEVEL FOUR-LEG SAPF

The basic operation of the proposed control method is shown in Fig.3. The nonlinear loads are constructed from three uncontrolled single-phase rectifiers. The DC voltage is compared with its reference value v_{dc}^{*}, in order to maintain the energy stored in the capacitors constant. The backstepping controller is used to regulate the error between the capacitor voltage and its reference. The output of backstepping controller of the DC voltage presents the reference of the equivalent capacitor current i_{dc}^{*}. The compensating currents are computed using the synchronous reference frame theory (SRF). Three backstepping controllers are used to regulate the injected SAPF currents at their references in αβo coordinate. The output signals from currents controllers are used for switching signals generation by the 3DSVM.

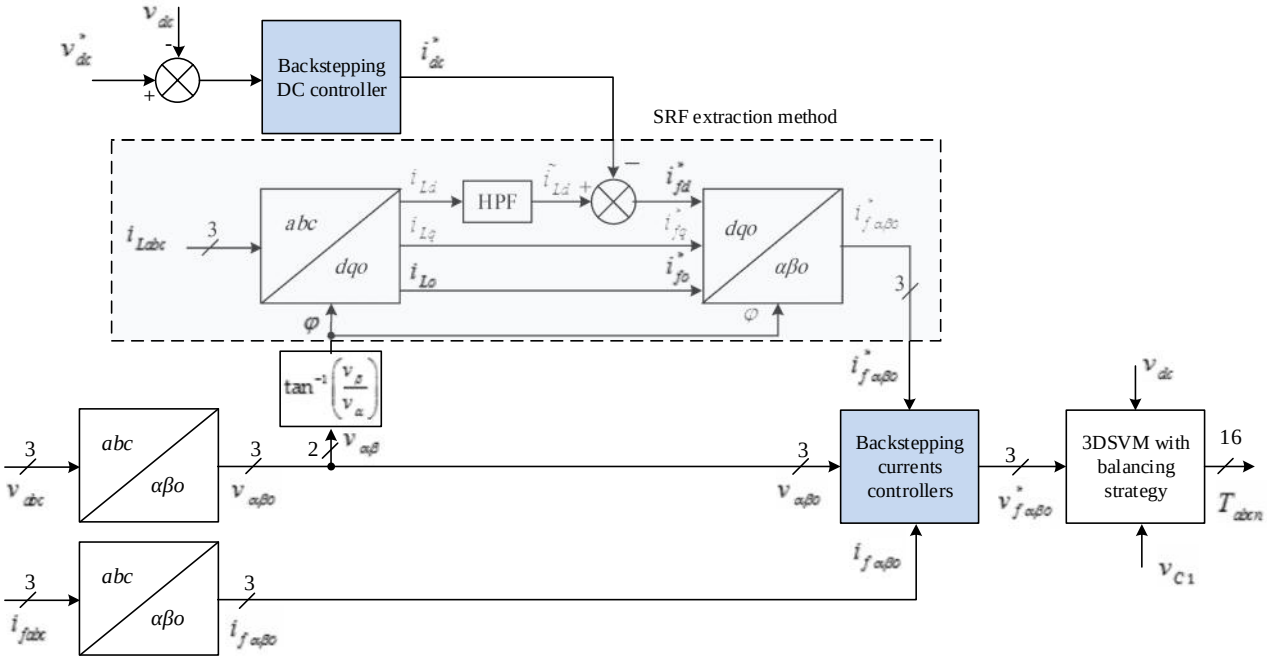


Fig.3. Backstepping control of three-level four-leg SAPF

3.1 Backstepping controller synthesis

There are four outputs to be controlled: DC capacitor voltage v_{dc} and injected SAPF current components $i_{f\sim}, i_f$ and i_{fo}. In order to ensure that each of the previously mentioned outputs follows its reference ($v_{dc}^*, i_{f\sim}^*, i_f^*$ and i_{fo}^* respectively), nonlinear controllers based on backstepping are synthesized in this section.

3.1.1 DC voltage controller synthesis

The synthesis of the DC voltage controller is based on the fourth equation of the system (6).

The first tracking error is defined as:

$$z_1 = v_{dc} - v_{dc}^* \tag{7}$$

Its derivative is:

$$\dot{z}_1 = \frac{i_{dc}}{C_{eq}} - \dot{v}^*_{dc} \tag{8}$$

The Lyapunov function is chosen as:

$$V_1 = \frac{1}{2} z_1^2 \tag{9}$$

The derivative of (9) is given by:

$$\dot{V}_1 = z_1 \dot{z}_1 = z_1 \left(\frac{i_{dc}}{C_{eq}} - \dot{v}^*_{dc} \right) \tag{10}$$

The equivalent capacitor current i^*_{dc} reference is selected such as the Lyapunov function $\dot{V}_1$ should be definite negative [38] as follow:

$$i^*_{dc} = C_{eq} \left(-k_1 z_1 + \dot{v}^*_{dc} \right) \tag{11}$$

Where: k_1 is a positive constant.

3.1.2 Current controller synthesis

From first three equations of system (6), the errors z_2, z_3 and z_4 are defined as:

$$\begin{aligned} z_2 &= i_{f\sim} - i^*_{f\sim} \\ z_3 &= i_f - i^*_f \\ z_4 &= i_{fo} - i^*_{fo} \end{aligned} \tag{12}$$

The Lyapunov functions are given by the following expressions:

$$\begin{aligned} V_2 &= \frac{1}{2} z_2^2 \\ V_3 &= \frac{1}{2} z_3^2 \\ V_4 &= \frac{1}{2} z_4^2 \end{aligned} \tag{13}$$

And consequently, their derivatives are given by:

$$\begin{aligned} \dot{V}_2 &= z_2\dot{z}_2 = z_2\left(\frac{1}{L_f}(v_{f\sim} - v_{\sim} - R_f i_{f\sim}) - \dot{i}^*_{f\sim}\right) \\ \dot{V}_3 &= z_3\dot{z}_3 = z_3\left(\frac{1}{L_f}(v_f - v - R_f i_f) - \dot{i}^*_f\right) \\ \dot{V}_4 &= z_4\dot{z}_4 = z_4\left(\frac{1}{L_f}(v_{fo} - v_o - R_f i_{fo}) - \dot{i}^*_{fo}\right) \end{aligned} \tag{14}$$

To make $\dot{V}_2 < 0$, $\dot{V}_3 < 0$ and $\dot{V}_4 < 0$, we must choose:

$$\begin{aligned} v^*_{f\sim} &= L_f\left(-k_2 z_2 + \dot{i}^*_{f\sim}\right) + v_{\sim} + R_f i_{f\sim} \\ v^*_f &= L_f\left(-k_2 z_2 + \dot{i}^*_f\right) + v + R_f i_f \\ v^*_{fo} &= L_f\left(-k_2 z_2 + \dot{i}^*_{fo}\right) + v_o + R_f i_{fo} \end{aligned} \tag{15}$$

Where: k_2, k_3 and k_4 are positive constants.

3.2 Synchronous Reference Frame Theory

The nonlinear load currents are transformed into the rotating frame dqo by the following expression:

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{Lo} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\phi & \cos\left(\phi - \frac{2\pi}{3}\right) & \cos\left(\phi - \frac{4\pi}{3}\right) \\ -\sin\phi & -\sin\left(\phi - \frac{2\pi}{3}\right) & -\sin\left(\phi - \frac{4\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{16}$$

Where: ϕ : is the angle of the PCC voltage vector $v^*_{\sim}$ projected in αβ plane. The angle ϕ is given by:

$$¤ = \tan 2^{-1}\left(\frac{v^{*}}{v^{*}_{\sim}}\right) \tag{17}$$

The nonlinear load current components i_{Ld} and i_{Lq} include AC and DC values and can be expressed as follows:

$$\begin{aligned} i_{Ld} &= \bar{i}_{Ld} + \tilde{i}_{Ld} \\ i_{Lq} &= \bar{i}_{Lq} + \tilde{i}_{Lq} \end{aligned} \tag{18}$$

The DC values $\left(\bar{i}_{Ld}, \bar{i}_{Lq}\right)$ of the i_{Ld} and i_{Lq} are originating from the positive-sequence component of the nonlinear load current. AC values $\left(\tilde{i}_{Ld}, \tilde{i}_{Lq}\right)$ are the ripple of the nonlinear load current components i_{Ld} and i_{Lq} [39].

For harmonic, reactive power compensation and balancing of unbalanced three-phase load currents, all of the nonlinear load current component i_{Lq} ($\bar{i}_{Lq}$ and $\tilde{i}_{Lq}$ components) and harmonic component $\tilde{i}_{Ld}$ of i_{Ld} are selected as compensation current references as follows:

$$\begin{bmatrix} i^{*}_{fd} \\ i^{*}_{fq} \end{bmatrix} = \begin{bmatrix} \tilde{i}_{Ld} - i^{*}_{dc} \\ i_{Lq} \end{bmatrix} \tag{19}$$

The signal i^{*}_{dc} is the reference of capacitor current obtained from the backstepping controller of DC voltage.

Since the zero-sequence current must be compensated, the reference of homopolair current is given as:

$$i^{*}_{fo} = i_{Lo} \tag{20}$$

The references currents can be written in αβo coordinate as follows:

$$\begin{bmatrix} i_{f\alpha}^{*} \\ i_{f\beta}^{*} \\ i_{fo}^{*} \end{bmatrix} = \begin{bmatrix} \cos\phi & -\sin\phi & 0 \\ \sin\phi & \cos\phi & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{fd}^{*} \\ i_{fq}^{*} \\ i_{fo}^{*} \end{bmatrix} \quad (21)$$

4. THREE DIMENSIONAL SPACE VECTOR MODULATION

In a three-level four-leg inverter, there are 81 possible switch combinations. The switch combinations are represented by ordered sets $(S_a S_b S_c S_n)$.

Where:

$$S_{a,b,c,n} \in \{0,1,2\} \quad (22)$$

Are the states of the inverter's leg.

As shown in Fig.4.a, all the 81 switching vectors can be sorted into thirteen layers. The diagram of space vectors can be divided into six sectors with every sector further divided into four prisms. As shown in Fig.4.b, the prisms 1 and 3 are formed by 7 tetrahedrons, while the prisms 2 and 4 are formed by 8 and 10 tetrahedrons respectively.

The 3DSVM technique can synthesize the reference voltage vector computed by backstepping currents controllers in three steps:

- Determination of the space vector location.
- Duration time calculation.
- Pulse generation.

3.2 Determination of the space vector location

The space vector location is determined in three sub-steps: (1) determining the sector number of where the reference voltage vector lies, (2) determining the number of prisms, and (3) determining the tetrahedron number of where the reference vector is located.

(a) (b)

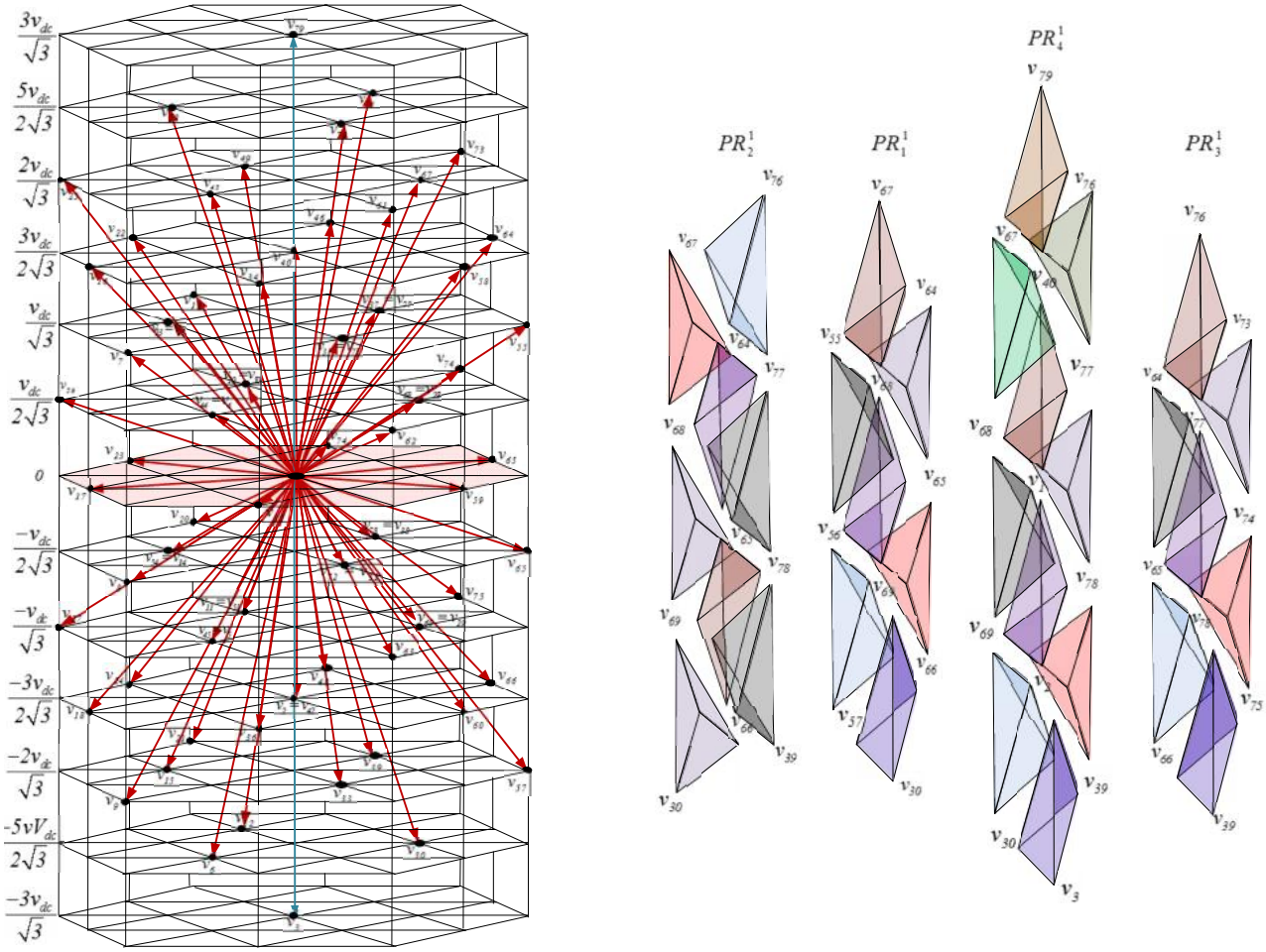


Fig.4. Three dimensional representations, (a): Switching voltages vectors in αβo coordinates, (b): Tetrahedrons in the first sector

4.1.1 Sector number computation.

The sector numbers are given by:

$$S_k = \text{ceil}\left(\frac{\bar{\ }}{\text{®}/3}\right), k \in \{1,2,3,4,5,6\} \quad (23)$$

Where *ceil* is the C-function that adjusts any real number to the nearest, but higher, integer.

$\bar{\ }$: is the angle of the v_f^* projected in αβ plane. The angle $\bar{\ }$ is given by:

$$\bar{} = \tan 2^{-1}\left(\frac{v_f^*}{v_{f\sim}^*}\right) \tag{24}$$

4.1.2 Prism identification

Reference vector v_f^* is projected on the axes of 60° coordinate system [40]. In each sector *k*, the normalized projected components are v_{f1}^{*k} and v_{f2}^{*k} given by (25). Fig. 5 shows the projection of v_f^* in the first sector.

$$\begin{aligned} v_{f1}^{*k} &= \frac{v_{f\sim}^*\ \cos(\bar{} - (k-1)\frac{®}{3})) - \frac{v_{f\sim}^*}{\sqrt{3}}\sin(\bar{} - (k-1)\frac{®}{3})}{\sqrt{\frac{2}{3}}\frac{v_{dc}}{2}} \\ v_{f2}^{*k} &= \frac{\frac{2}{\sqrt{3}}v_{f\sim}^*\ \sin(\bar{} - (k-1)\frac{®}{3})}{\sqrt{\frac{2}{3}}\frac{v_{dc}}{2}} \end{aligned} \tag{25}$$

Where: $v_{f\sim}^*$ is the projected vectror of v_f^* in αβ plane.

$$v_{f\sim}^* = \sqrt{v_{f\sim}^{*2} + v_f^{*2}} \tag{26}$$

In order to identify the prism where the required reference is located, the following integers are used:

$$\begin{aligned} l_1^k &= \text{int}\left(v_{f1}^{*k}\right) \\ l_2^k &= \text{int}\left(v_{f2}^{*k}\right) \end{aligned} \tag{27}$$

Where the *int*() function returns the nearest integer that is less than or equal to its argument. The prism number is obtained according to the value of l_1^k and l_2^k , as shown in Table 1:

Table 1. Prism identification in each sector S_k, where: PR_i^k is a prism number *1* located in sector S_k

l_1^k	l_2^k	PR_i^k
0	0	PR_1^k (if $v_{f1}^{*k} + v_{f2}^{*k} < 1$)
		PR_2^k (if $v_{f1}^{*k} + v_{f2}^{*k} \geq 1$)
1	0	PR_3^k
0	1	PR_4^k

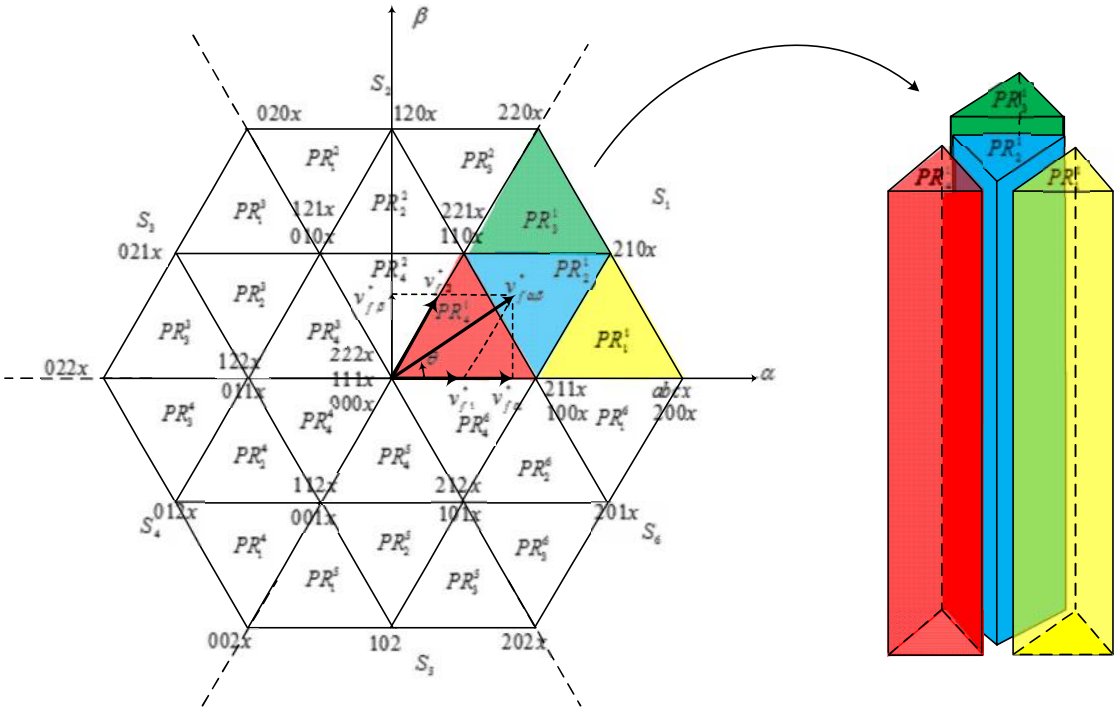


Fig.5. Space voltage vectors for a three-level four-leg inverter on αβ plan

4.1.3 Tetrahedron identification

As shown in Fig. 5, each tetrahedron is limited by four planes; two plants are limited by the prism that contains the tetrahedron, so just the top and the bottom planes must be determined for identify the tetrahedron. Each plane is created by three switching vectors. For example, the

localization condition of tetrahedron 1 in the prism 1 of the first sector numbered as TeT_j^i (i=1 for prism 1 and j=1 for tetrahedron 1) is given by:

$$\begin{aligned} v_{fo}^* &\le -v_{f\sim}^* + \sqrt{\frac{3}{2}} v_{dc} \\ v_{fo}^* &> \frac{v_{f\sim}^*}{2} + \frac{\sqrt{3}}{2} v_f^* \end{aligned} \tag{28}$$

4.2 Duration time calculation

After determining the target tetrahedron of the reference voltage vector, the four adjacent switching vectors will be used to express the average value of the reference voltage vector as follow:

$$\begin{aligned} v_1 t_1 + v_2 t_2 + v_3 t_3 + v_4 t_4 &= v_f^* T_s \\ t_1 + t_2 + t_2 + t_4 &= T_s \end{aligned} \tag{29}$$

Where T_s is the switching period, v_1, v_2, v_3 and v_4 are the four switching vectors adjacent to the reference voltage vector, and t_1, t_2, t_3 and t_4 are their calculated on-duration time intervals respectively.

Expression (29) can be decomposed in the *αβo* coordinates system as follows:

$$\begin{bmatrix} v_{1\sim} & v_{2\sim} & v_{3\sim} & v_{4\sim} \\ v_1 & v_2 & v_3 & v_4 \\ v_{1o} & v_{2o} & v_{3o} & v_{4o} \\ 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} t_1 \\ t_2 \\ t_3 \\ t_4 \end{bmatrix} = \begin{bmatrix} v_{f\sim}^* T_s \\ v_f^* T_s \\ v_{fo}^* T_s \\ T_s \end{bmatrix} \tag{30}$$

4.3 DC-Capacitors voltages balancing based on minimum energy property

In the three-level four-leg inverter, the voltages of the two series-connected DC-link capacitors must be confined to $v_{dc}/2$. The DC voltage backstepping control regulates only the total DC voltage. For this reason, the DC capacitor voltages are kept equals using 3DSVM

that takes advantages of redundant switching states to counteract the DC voltages drift phenomenon [41].

The electrical energy stored in the chain of DC-link capacitors is given by:

$$E = \frac{C}{2}(v_{C1}^2 + v_{C2}^2) \tag{31}$$

The adopted control method should minimize the quadratic cost function *J* associated with voltage deviation of the DC-capacitors. The cost function is defined as follows:

$$J = \frac{C}{2}(\Delta v_{C1}^2 + \Delta v_{C2}^2) \tag{32}$$

Where:

$$\Delta v_{Cj} = v_{Cj} - v_{dc}^* / 2, \quad j = 1,2$$

The mathematical condition to minimize *J* is:

$$\frac{dJ}{dt} = \Delta v_{C1} i_{C1} + \Delta v_{C2} i_{C2} \leq 0 \tag{33}$$

Where i_{Cj} (j =1,2) is the current through capacitor C_j. These currents are affected by the DC-side intermediate branch currents, i_0 and i_1. These currents can be calculated if the switching states used in the switching pattern are known. Thus, it is advantageous to express (33) in terms of i_0, and i_1. The DC-capacitor currents are expressed as:

$$\begin{aligned} i_{C1} &= i_1 \\ i_{C2} &= i_1 + i_0 \end{aligned} \tag{34}$$

By substituting i_{C2} and i_{C1} given by (34) in (33), the condition to achieve voltage balancing is deduced as:

$$\Delta v_{C1} i_1 + \Delta v_{C2}(i_1 + i_0) \le 0 \quad (35)$$

When the DC link voltages v_{C1} and v_{C2} are close to their reference $v_{dc}^{*}/2$, the following condition is verified :

$$\Delta v_{C1} + \Delta v_{C2} = 0 \quad (36)$$

Using (36), the equation (35) can be written as:

$$\Delta v_{C2} i_0 \le 0 \quad (37)$$

Applying the averaging operator, over one sampling period, to (37) results in:

$$\frac{1}{T}\int_{kT}^{(k+1)T} (\Delta v_{C2} i_0) dt \le 0 \quad (38)$$

Assuming that sampling period *T*, is adequately small as compared to the time interval associated with the dynamics of capacitor voltages. These letters can be assumed to remain constant over one sampling period [41] and (38) is consequently simplified to:

$$\Delta v_{C2}(k)\bar{i}_0 \le 0 \quad (39)$$

Where $\Delta v_{C2}(k)$ is the voltage drift at sampling period, and $\bar{i}_0$ is the averaged value of the i_0.

The relationship between the DC-intermediate branch current i_0 and AC-currents (i_{fa}, i_{fb} and i_{fc}) for different switching states is required.

The current $\bar{i}_0$ should be computed for different combinations of adjacent redundant switching states over a sampling period and the best combination which minimizes (39) is selected.

6. SIMULATION RESULTS AND DISCUSSION

To validate the performance of the three-level four-leg SAPF compensator, computer simulations are performed on a three-phase four-wire power system under various nonlinear loads and source voltages conditions, including:

- Balanced nonlinear load condition.
- Unbalanced nonlinear load condition.
- Unbalanced source voltages.
- Distorted source voltages.

The parameters used in simulation are gathered in Table.2.

Table 2. System parameters

Capacitance of each capacitor	**5 mF**
DC bus voltage reference	800 V
Coupling impedance R_f ,L_f	0.1 mΩ, 0.1 mH
RMS source voltage and frequency	220 V, 50 Hz
Source parameters R_s ,L_s	1 mΩ, 1 mH
Line parameters R_{ch} ,L_{ch}	1 mΩ, 1 mH
Load characterisitics R_l ,L_l	5 Ω, 10 mH
Parameters of unbalanced load R , L	5 Ω, 10 mH

6.1 Balanced nonlinear load and source voltages condition

Figs (6), (7) and (8) present the source current of the first phase and its harmonic spectrum before and after compensation of three-level four-leg SAPF using backstepping and conventional PI controllers, respectively.

Fig. 6 illustrates that the source current before compensation is distorted, and its total harmonic distortion (THD) is equal to 17.08 % (see Fig. 6.b).

It can be shown from Figs. 7 and 8, that the proposed backstepping controller allows the four-leg SAPF to mitigate the source current harmonics and offer better THD than conventional PI controller (0.34% using backstepping and 2.09% using PI controller).

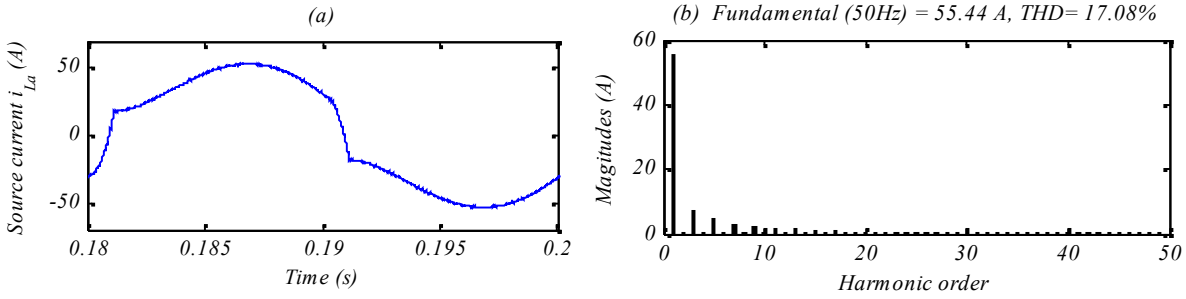


Fig.6. (a) Source current before harmonics compensation, (b) Its harmonic spectrum

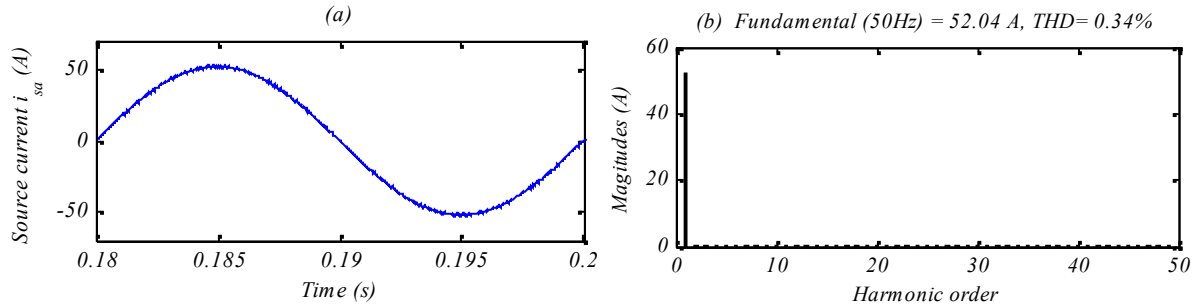


Fig.7. (a) Source current after harmonics compensation using backstepping controller, (b) Its harmonic spectrum

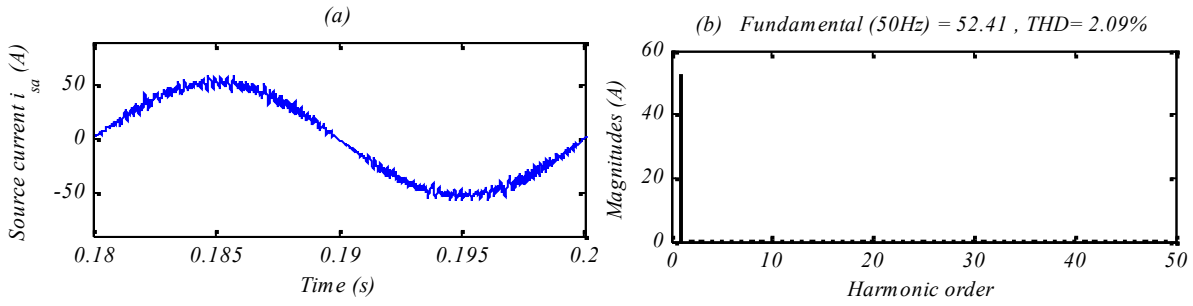


Fig.8. (a) Source current after harmonics compensation using PI controller, (b) Its harmonic spectrum

6.2 Unbalanced nonlinear load condition

Figs. 9 and 10 present the dynamic behaviour of the three-level four-leg SAPF using backstepping and PI controllers respectively. After 0.15s, an additional load is added in single-phase diode bridge rectifier in phase (b) in order to induce an unbalanced nonlinear load.

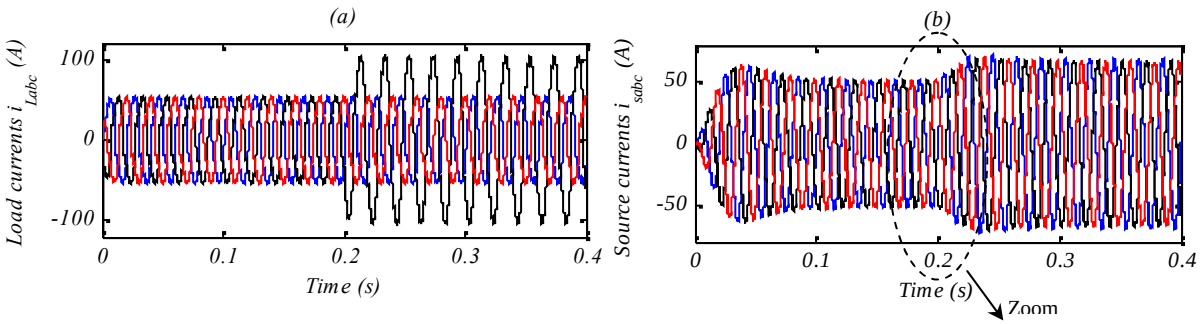
From Figs. 9.b and 10.b, the nonlinear load currents are distorted and unbalanced after 0.2s, while the source currents are forced to have a balanced and sinusoidal shape in both control techniques (see Figs 9.a and 10.a).

As shown in Figs 9.c and 10.c, the neutral current is almost cancelled with a low ripple in case where the backstepping control is applied (2.15% for backstepping and 28.5% for PI).

The phase (a) of source current and its corresponding phase voltage are shown for illustration in Figs 9.d and 10.d. It can be observed that the unity power factor operation is successfully achieved.

Fig. 10.e shows the DC voltage in case of conventional PI controller, where the performance suffers from critical overshoots. On the contrary, the proposed backstepping control enhance the performance of the DC voltage control loop, whitch maintains it close to its reference value without overshoots (see Fig. 9.e).

It can be observed from Figs. 9.g and 10.g that the DC capacitor voltages are balancing at their reference values with small ripple around the balance point with both control methods (0.25% before 0.2s and 1.5% after 0.2s), which confirms the effectiveness of the 3DSVM equipped with the proposed balancing strategy.



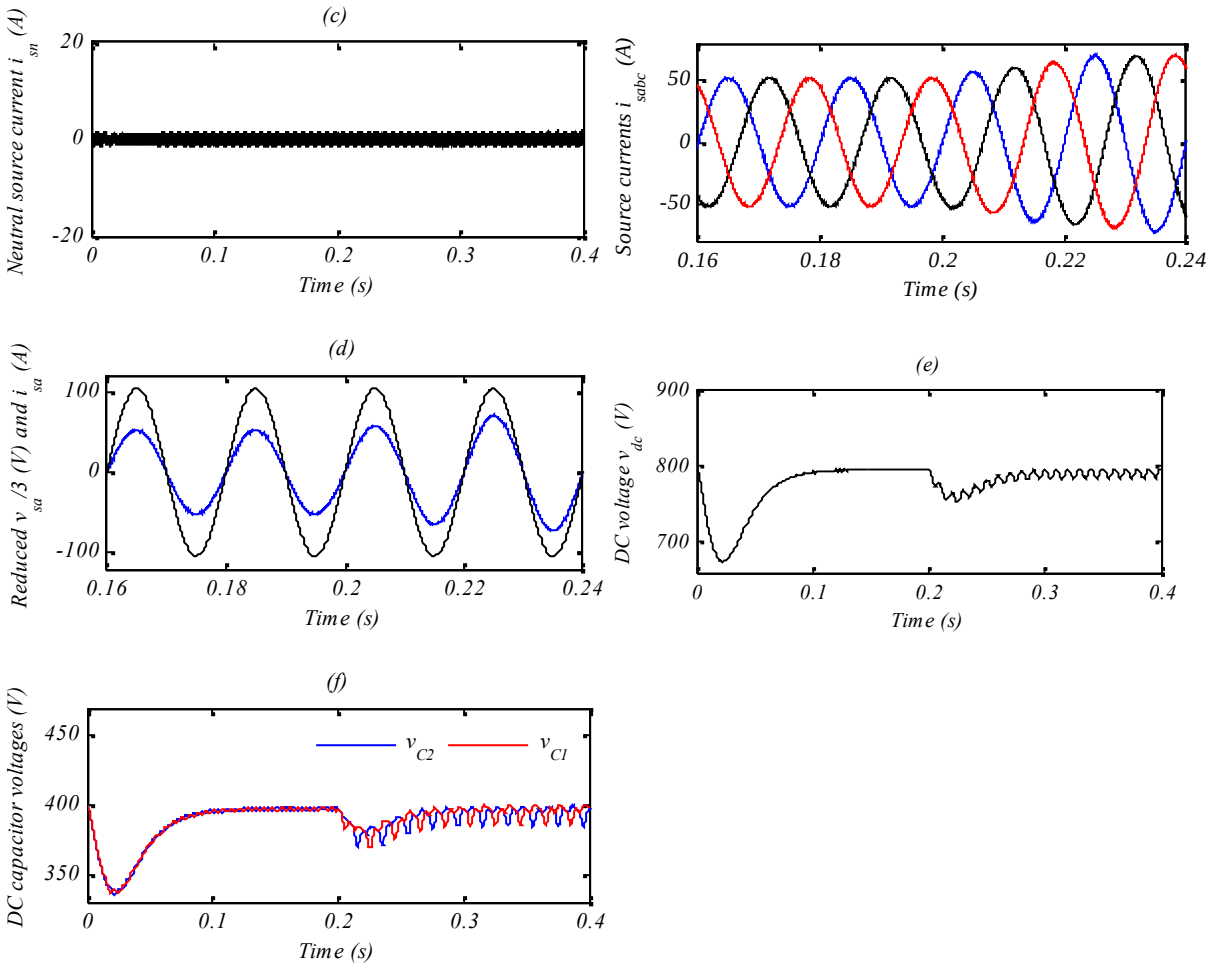
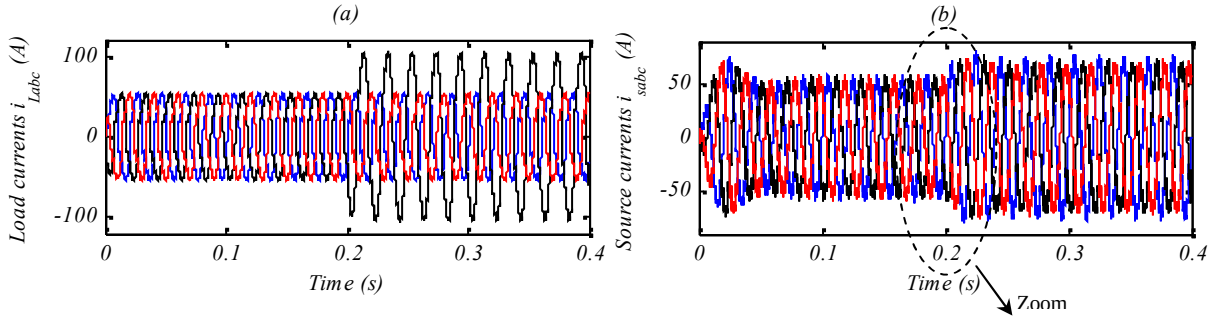


Fig.9. Simulation results of the proposed three-level four-leg SAPF using backstepping controller under balanced load



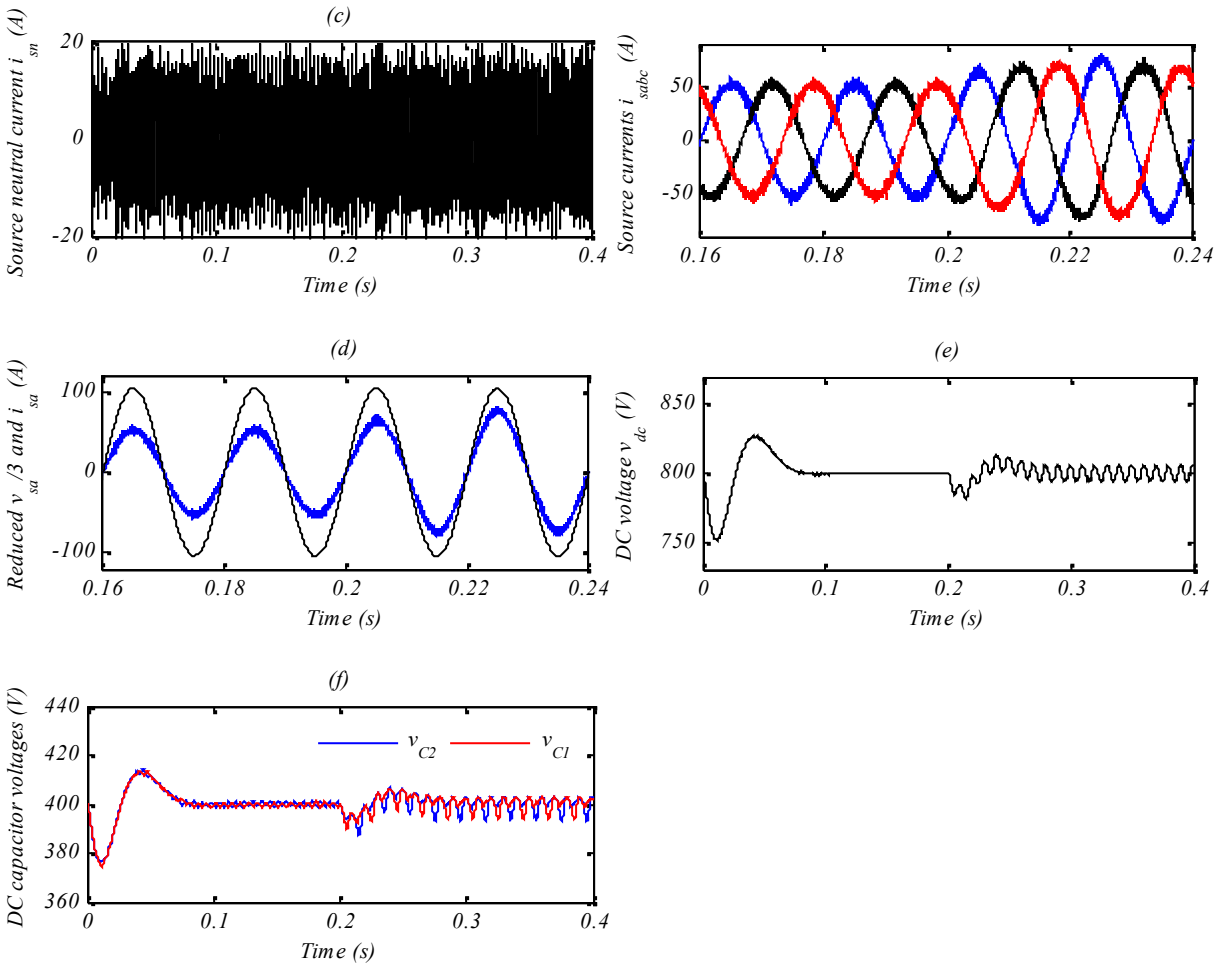


Fig.10. Simulation results of the proposed three-level four-leg SAPF using PI controller under balanced load

6.3 Unbalanced source voltages condition

The simulation results with the backstepping and PI controller under unbalanced source voltages are shown in Figs. 11 and 12, respectively. In order to create this operating condition, the magnitude of source voltage of phase (a) is 20% smaller than source voltage of phase (b) and phase (c).

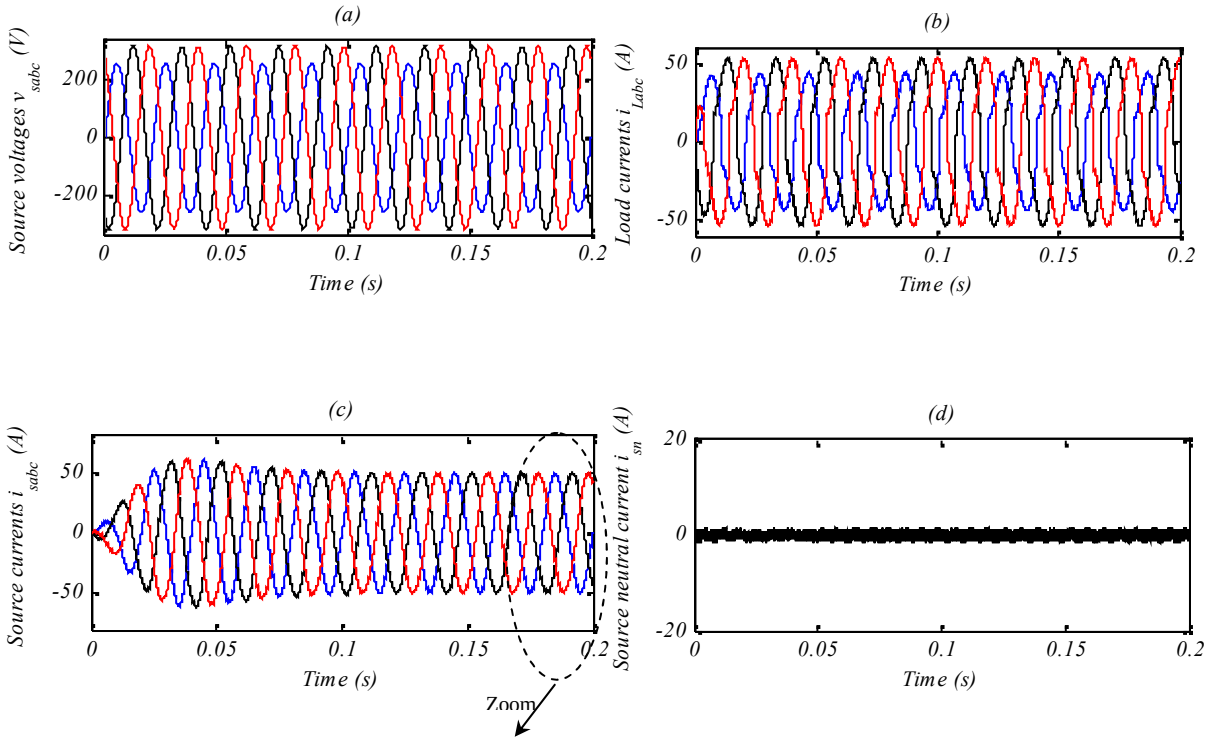
As shown in Fig. 11.a and 12.a, the unbalanced source voltages, leads to unbalance in the nonlinear load currents (see Figs. 11.b and 12.b). The source currents, after the compensation, can be viewed from Figs. 11.c and 12.c. The source currents now become free from unwanted harmonics and close to balanced case. The source neutral currents are

depicted in Figs. 11.d and 12.d, a better neutral current compensation with low ripple is obtained when the proposed control is used.

The source current is in phase with corresponding source voltage (see Figs. 11.e and 12.e), which means that the reactive power is successfully compensated.

It is also observed from Figs. 11.f and 12.f that the DC voltage of SAPF is maintained close to the reference value under unbalanced source voltage, and without overshoots with the proposed control method. The DC capacitor voltages tend to be equal independently to the used control method, thanks to the 3DSVM with its balancing strategy (see Figs 11.g and 12.g).

The harmonic spectrums of the source current after compensation are illustrated in Fig.13. It results that the four-leg SAPF decreases the THD in the source currents under this disturbances to 4.36% with PI controller. However, with backstepping controller, the THD is increased to 3.26% which proves the effectiveness of the proposed nonlinear controller.



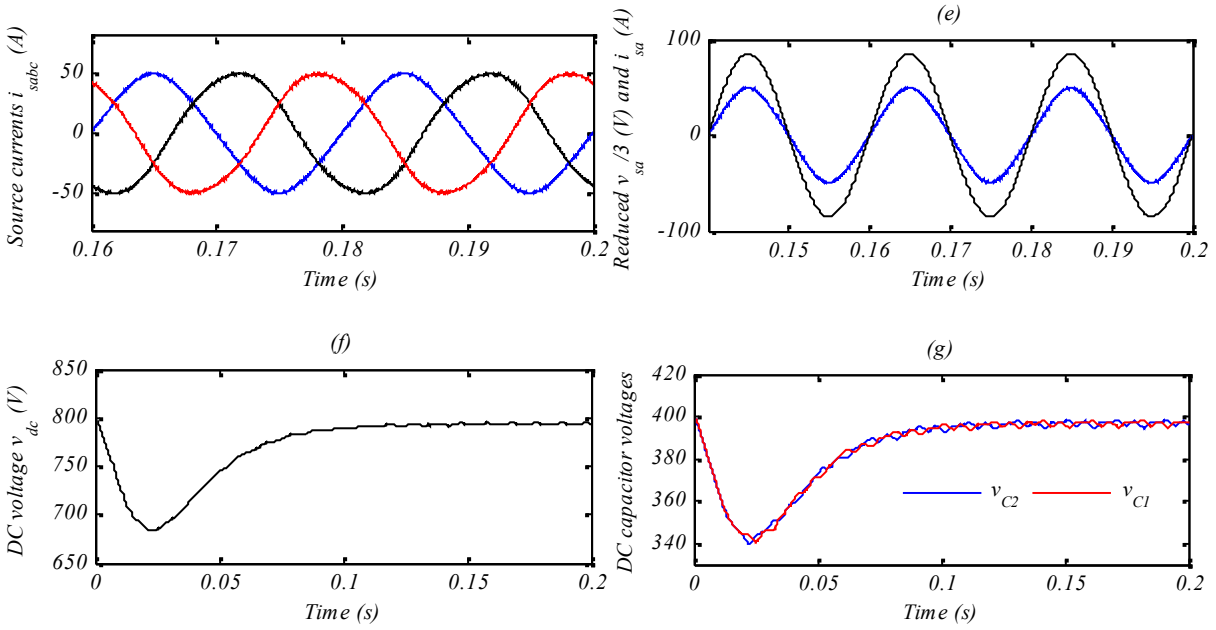
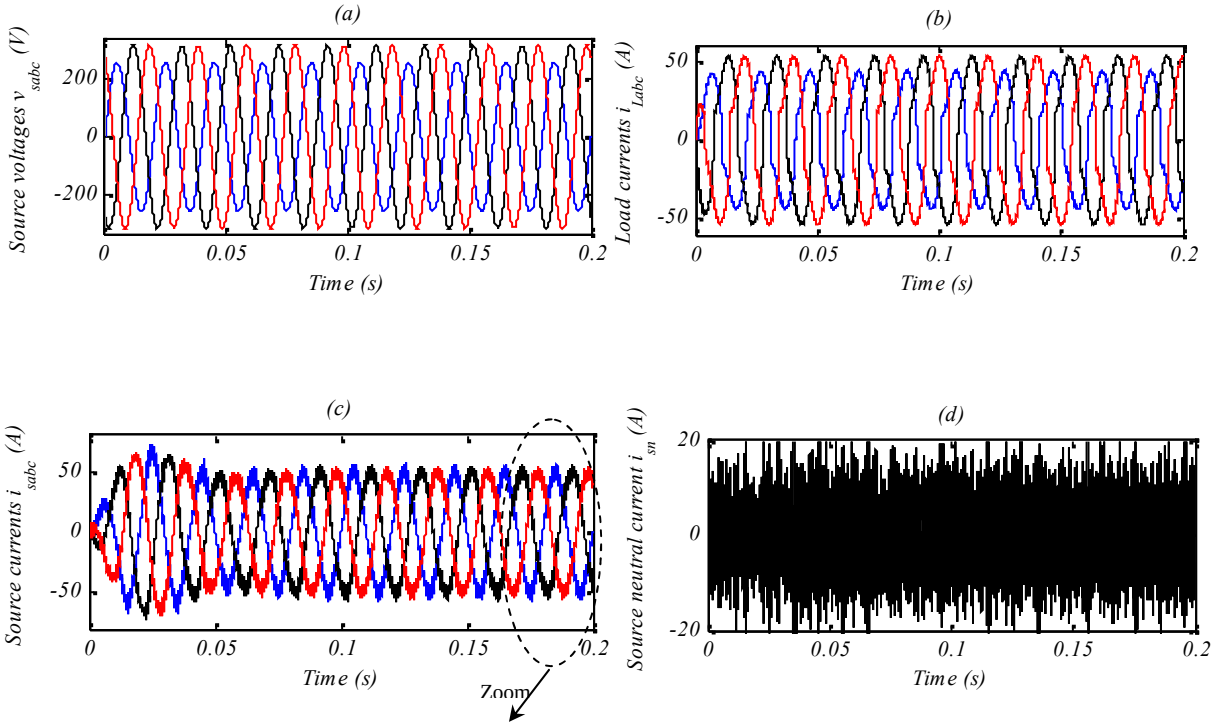


Fig.11. Simulation results of the proposed three-level four-leg SAPF using backstepping controller under unbalanced source voltage



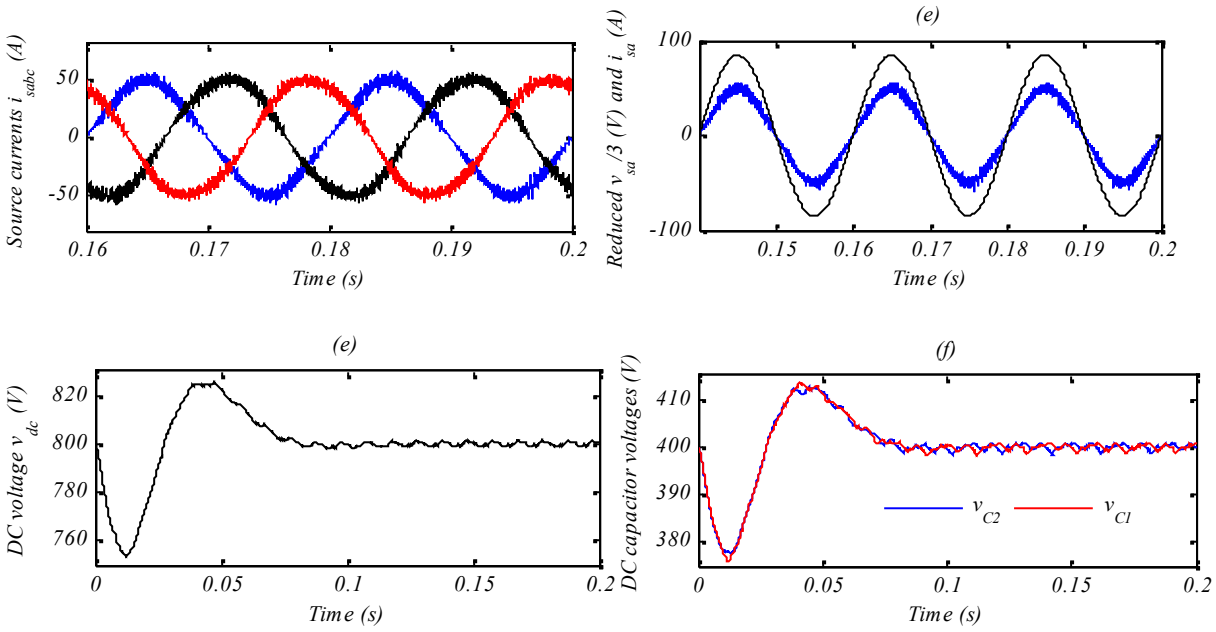


Fig.12. Simulation results of the proposed three-level four-leg SAPF using PI controller under unbalanced source voltage

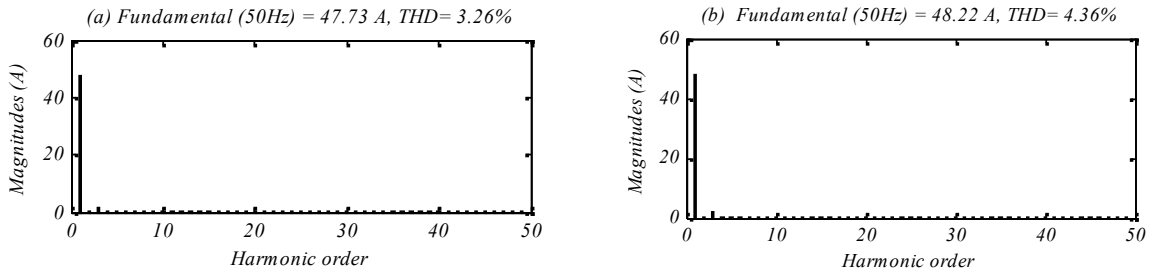


Fig.13. Frequency spectrum of source current under unbalanced source voltage, (a) Using backstepping controller, (b) Using PI controller

6.3 Distorted source voltages condition

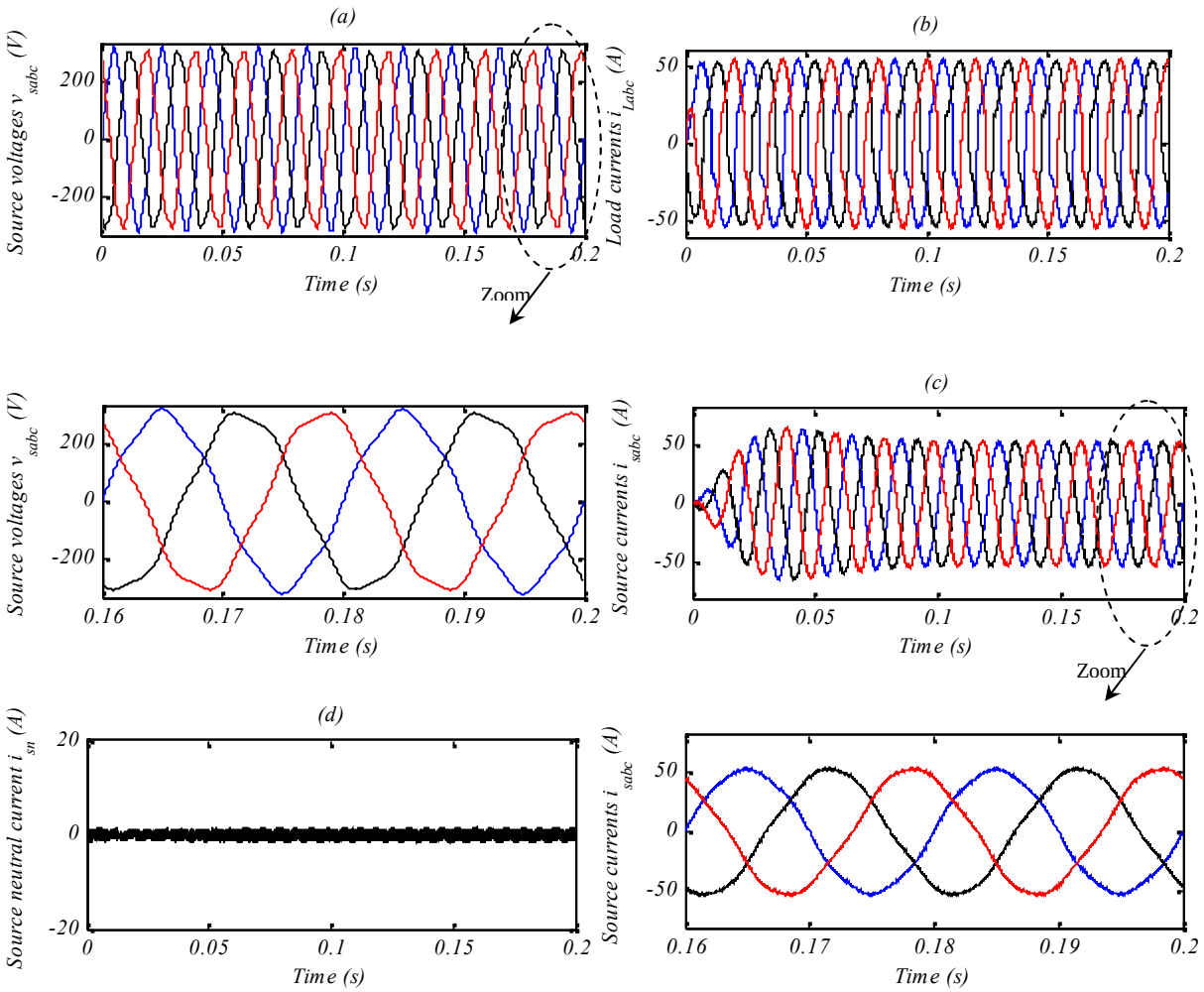
One of the assumptions is that the source voltage is sinusoidal and balanced. However, in real systems, source voltage can be temporary, or permanently distorted by faults, short circuits, connections and disconnections of large loads, nonlinear loads, etc. Usually, it leads to the presence of source voltage harmonics. One of the main disturbances is the presence of source voltage harmonics of order 5, 7 and 11.

Figs. 14 and 15 show the waveforms in which a fifth harmonic voltage component of 5% is intentionally superimposed on the fundamental source voltages for proposed SAPF using

backstepping and PI respectively. It is observed that the source currents are sinusoidal, balanced and in phase with the phase voltages, which mean that the unity power factor is successfully achieved. The neutral current is practically cancelled with low ripple in case of backstepping control.

The DC voltage is adequately controlled around its reference value and without overshoots when the backstepping control is used. It is possible to see also how the voltage across each capacitor remains constant under this operating condition.

As shown in Fig. 16 the total harmonic distortion of the source current is 4.57% with PI and 3.77% with backstepping controller, which proved once the effectiveness of the proposed control method.



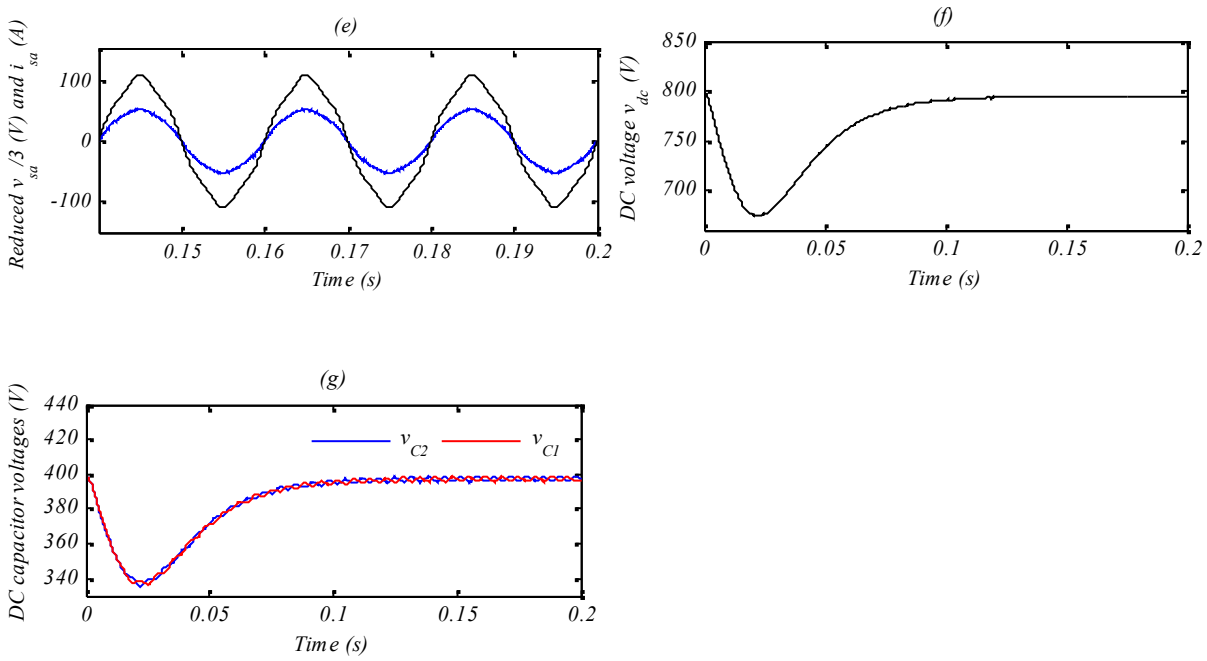
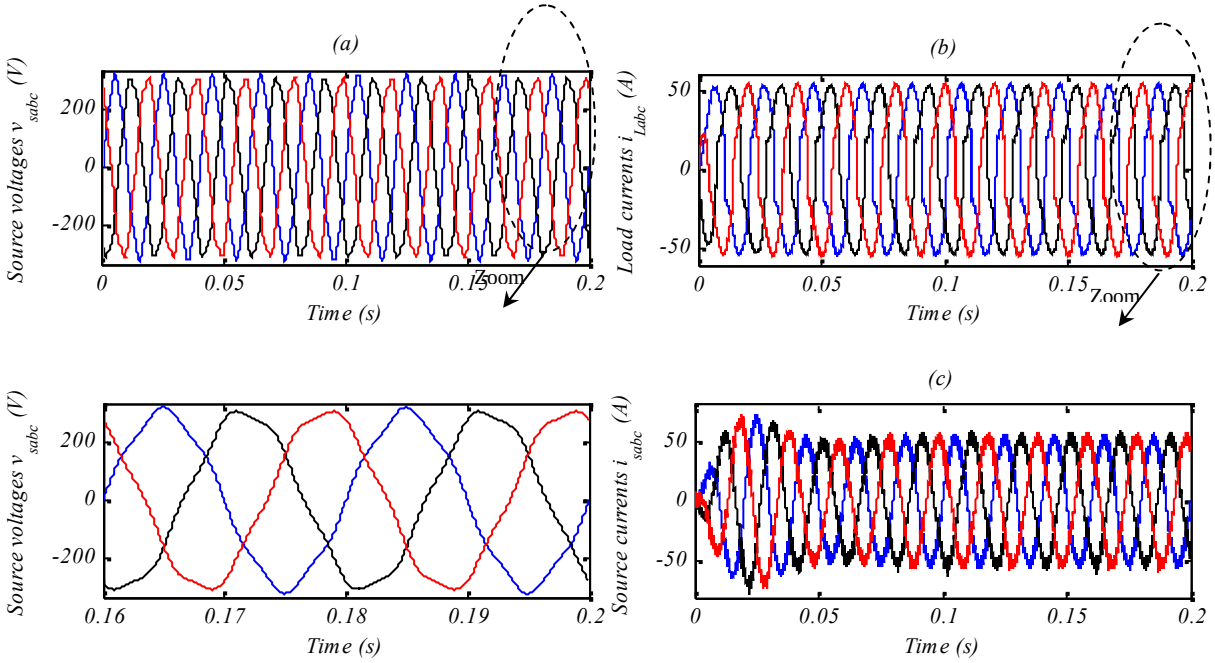


Fig.14. Simulation results of the proposed three-level four-leg SAPF using backstepping controller under distorted source voltage



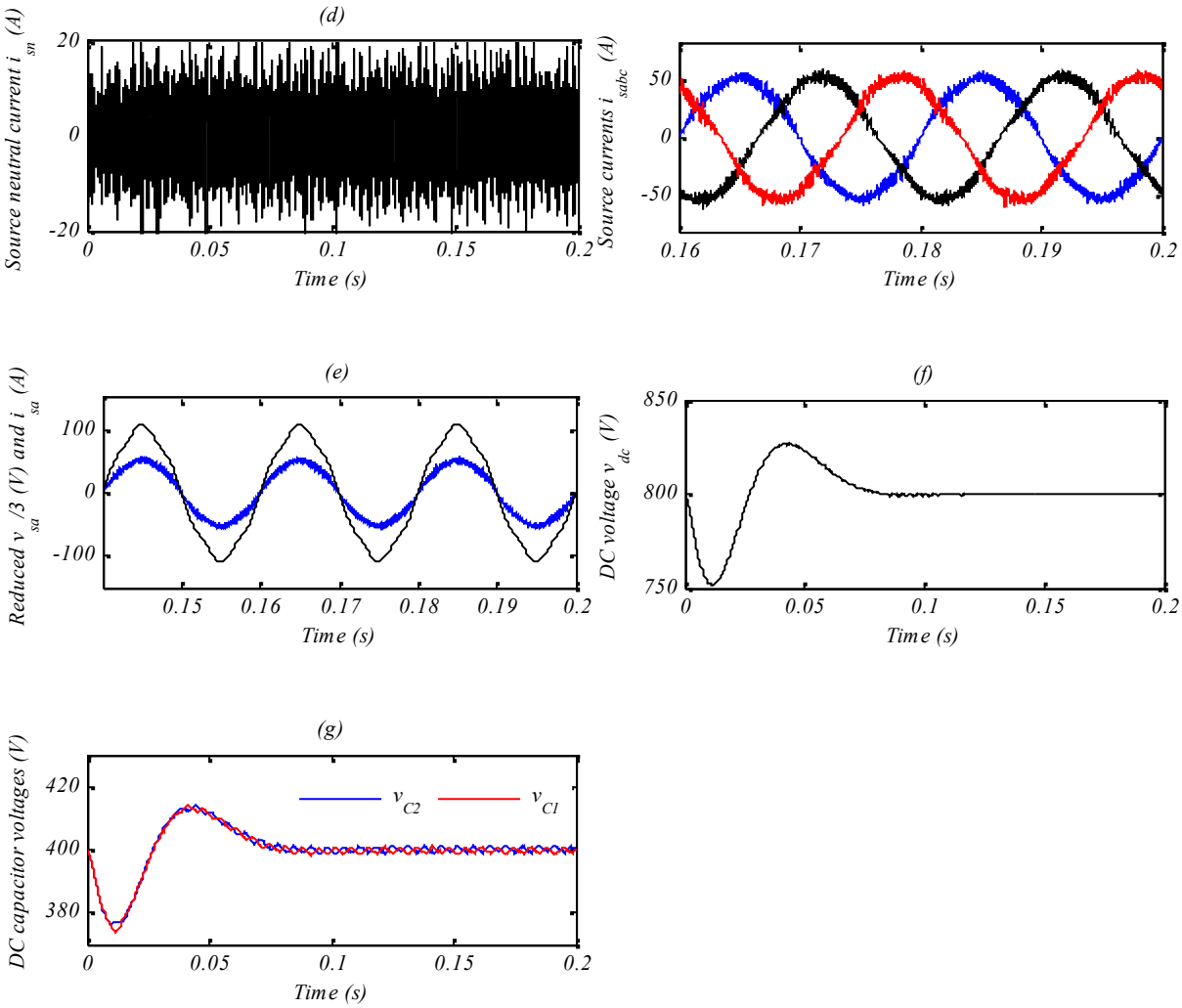


Fig.15. Simulation results of the proposed three-level four-leg SAPF using PI controller under distorted source voltage

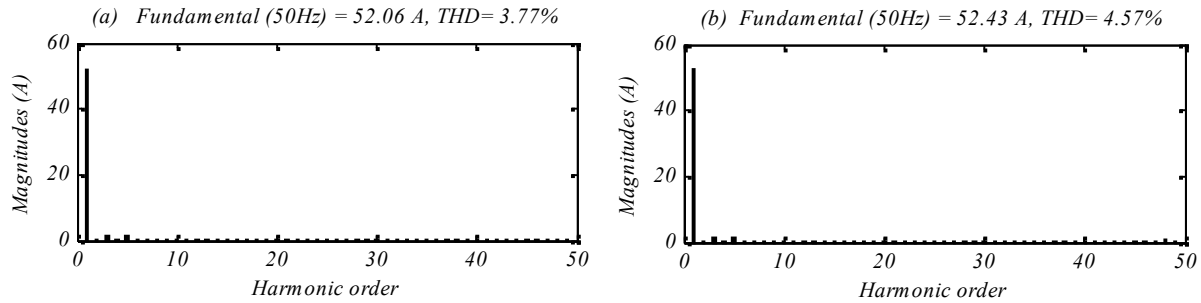


Fig.16. Frequency spectrum of source current under distorted source voltage, (a) Using backstepping controller, (b) Using PI controller

7. CONCLUSION

In the aim to enhance power quality in four-wire system, this paper proposes a backstepping control of three-phase three-level four-leg SAPF. The performances of the active power filtering system based on backstepping controller are analyzed and compared with conventional controller under different disturbed operating conditions.

The computer simulation has verified the effectiveness of the proposed control scheme. The simulation results prove that the following objectives have been successfully achieved even under unbalanced nonlinear load and non-ideal source voltage conditions.

- Current harmonics filtering.
- Reactive power compensation.
- Source currents balancing.
- Elimination of excessive neutral current with low ripple.
- High performance under both dynamic and steady state operations.

The voltage balancing control of DC capacitors of the three-level four-leg inverter is achieved using 3DSVM with balancing strategy, which is based on the effective use of the redundant switching states of the inverter voltage vectors. The simulation results show that the 3DSVM with balancing strategy can guarantee balancing of the DC capacitor voltages under all operating conditions and independently to the used control method.

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