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A PMSM CURRENT CONTROLLER SYSTEM ON FPGA PLATFORM

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ABSTRACT

Permanent magnet synchronous motor (PMSM) has gained more interest recently in industrial applications. Digital hardware solutions such as field programmable gate arrays (FPGAs) are the most preferred methods for controlling PMSM drivers. This paper presents an implementation of a current control system for PMSM based on FPGA. Encoder-based speed and position detection method has been used in proposed hardware. The whole system has been modeled and simulated in system level using MATLAB/SIMULINK. Hardware architecture for all computational blocks is implemented using Verilog HDL. The hardware architecture has been successfully synthesized and implemented on Altera Cyclone II FPGA. Proposed system architecture and computational blocks are described and system level and RTL simulation results are presented. Simulation results show that the total computation cycle time of implemented system on Altera Cyclone II FPGA is 456ns.

Keywords: PMSM, FPGA, Incremental encoder, CORDIC, Hysteresis Current Control.

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1. INTRODUCTION

1.1. PMSM current control system

PMSM has been used in many automation fields because of many advantages over induction motors such as superior power density, high performance motion control with fast speed and better accuracy. Several methods have been proposed in order to control PMSM based on electric current measurements. Programmable hard-wired feature, fast computation ability, shorter design cycle, embedded processor usage capability and high hardware density have made FPGAs more suitable for implementation of digital control systems [1]. FPGAs are the most preferred methods for controlling PMSM driverscomparing to software solutions based on DSPs or microcontrollers [2-7].

Angular measurement of the rotor position is an essential parameter in PMSM control applications. Shaft encoders (incremental, absolute, sine...) and electromagnetic resolvers are two common sensors that are used for angular measurements. Electromagnetic resolvers are absolute angle transducers, providing two output signals that always allow the detection of the absolute angular position [8,9]. The main disadvantages of the resolver based system are high cost and more complexity. The output of the resolver is an analog signal that makes the need for analog circuitry for filtering and also A/D conversion that makes whole system more complicated and more expensive. Encoders have digital outputs and are easily interfaced to digital hardware. There are two types of encoders that are used in these applications: Incremental type and absolute type. Incremental encoders have simpler structure but they are relative position sensors, on the other hand absolute encoders are complicated and expensive.

The general structure of the control system is depicted inFig.1. Encoder processing unit measures speed and position of rotor. Hysteresis current controller consists of DQ-ABC block and three-phase hysteresis block. Detailed information about the hardware blocks in this diagram is presented in the following sections.

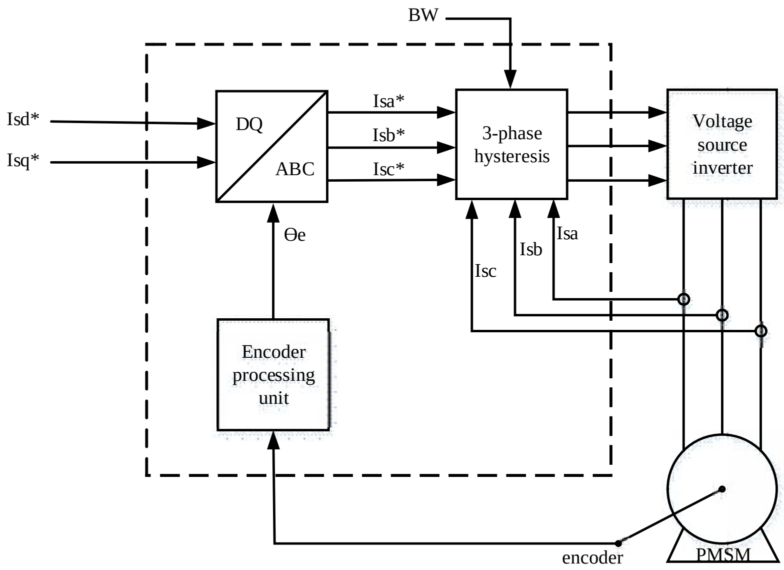


Fig.1. General block diagram of PMSM current control system

1.2 Encoder processing unit

The knowledge of position and speed of the rotor is an important parameter in PMSM drives [10,11]. Incremental encoders are commonly used as position transducers in sensored drives in order to measure rotational speed and position of rotor. Incremental encoder generates a definite number of pulses in one revolution of the encoder that is coupled to the rotor [12]. The most common type of incremental encoder uses two output channels (A and B) to sense position and direction of rotation, as shown in Fig.2. A third output channel (Z) that called zero or reference signal, generates a single pulse per revolution.

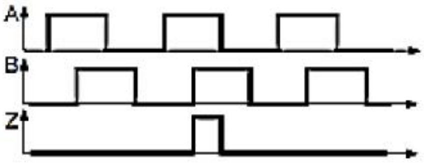


Fig.2. Output signals generated by Incremental Encoder

The angular position (θ) of encoder based system is obtained by counting the number of generated encoder pulses according to the direction of rotation and multiplying it by the angular step (θ_p) of the encoder [13].

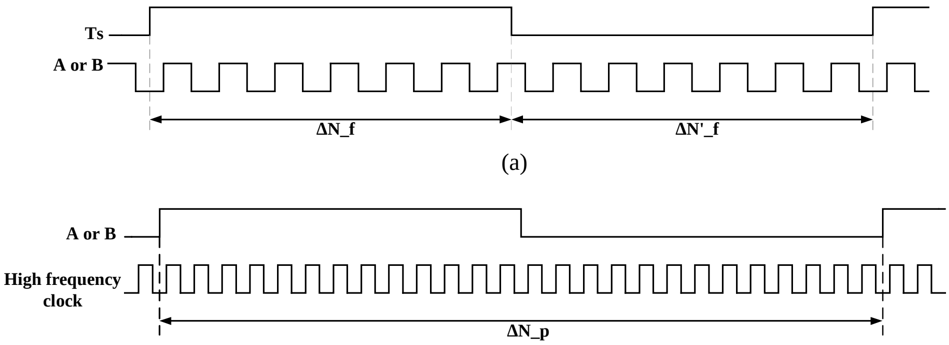
$$\theta = \theta p\left[\sum_{i} Ni - \sum_{j} Nj\right] = \theta p N \tag{1}$$

As the shaft of encoder rotates faster, the pulse frequency increases accordingly. The output pulses can be transformed into speed units by measuring their frequency by an appropriate scale factor. (Fig.3)

The angular speed is determined by the expression:

$$\omega = \frac{d\theta}{dt} \cong \frac{\Delta\theta}{\Delta t} = \frac{\theta p \Delta N}{Ts} \tag{2}$$

The frequency based speed calculator produces relatively small errors at high speed because the number of pulses from the encoder in the measurement interval is high ($\varepsilon\varepsilon \propto \frac{1}{\Delta N}$). However this method has large error at lower speeds. In case of lower rotation speeds, time period measurement method has better performance. In this method the time interval between two sequential encoder pulse is measured using a high frequency clock timer as is shown in Fig.3[14].



(a)

(b)

Fig.3. Methods of speed calculation a. based on frequency b. based on period

The angular speed in this case is determined by the expression:

$$\omega = \frac{d\theta}{dt} \cong \frac{\Delta\theta}{\Delta t} = \frac{\theta p}{nThf} \tag{3}$$

On the other hand, period measurement method has larger errors at high rotation speeds. The error of this method is inverse proportional to the number of pulses which counted from high frequency clock ($\varepsilon \propto \frac{1}{n}$). In this paper we have combined these two methods to have acceptable performance both at high and low speeds of rotation. The proposed hardware structure for Encoder Processing Unit is shown inFig.4. This module has four main parts: frequency based speed calculator, period based speed calculator, position detector and direction detector. The direction detector block identifies the direction of the rotation. The counter CCW will be enabled when the direction of the shaft rotation is counterclockwise, and will be count the encoder pulses A. If the direction of the shaft rotation is clockwise, the counter CW will be enabled and will count the pulses B.

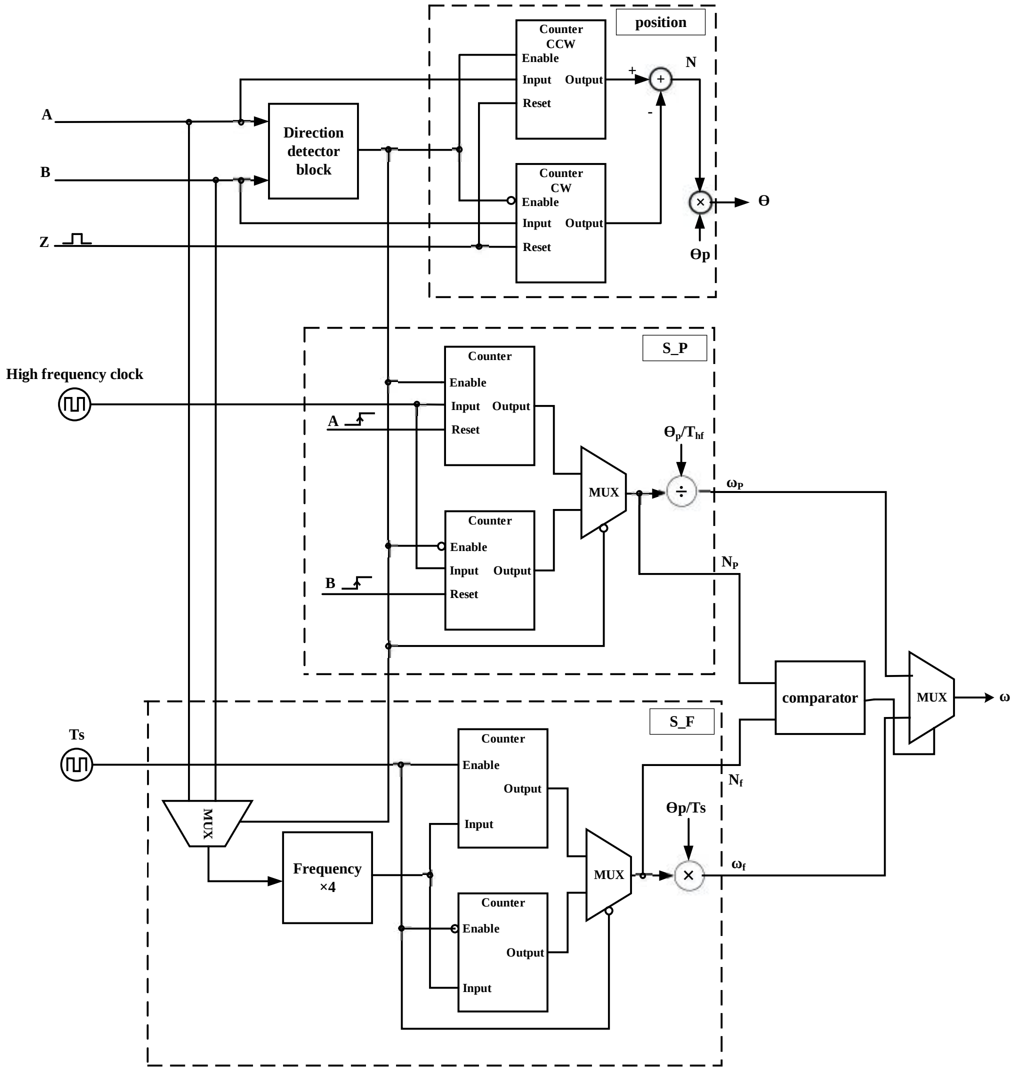


Fig.4. Hardware structure of proposed Encoder Processing Unit

1.3 Current controller

The main parts of current controller are DQ-ABC coordinate transformation module and three-phase hysteresis regulator .The DQ-ABC module consists of inverse Park transformation and inverse Clarke transformation. The output of the DQ-ABC module is the three-phase reference current according to the DQ reference current and the electrical position of the rotor.Three-phase hysteresis regulator module generates PWM signals according to the three-phase reference currents and the stator three-phase current.

1.3.1 DQ_ABC module

The DQ-ABC module can be implemented by combining the equations of Inverse Park and Inverse Clarke transformations. Three-phase current references for DQ-ABC module are expressed as:

$$I_a^* = I_d^* \cdot \sin\left(\theta + \frac{\pi}{2}\right) + I_q^* . \sin(\theta + \pi) \quad (4)$$

$$I_b^* = I_d^* \cdot \sin\left(\theta + \frac{11\pi}{6}\right) + I_q^* . \sin\left(\theta + \frac{\pi}{3}\right) \quad (5)$$

$$I_c^* = -(I_a^* + I_b^*) \quad (6)$$

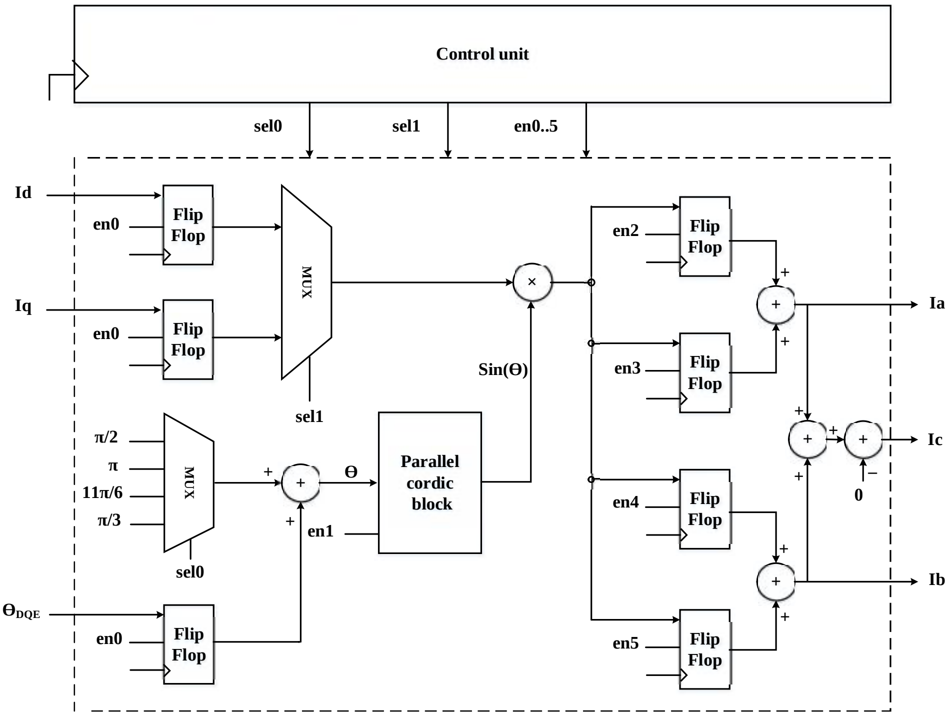


Fig.5. Block diagram of the DQ-ABC module

Block diagram of proposed DQ-ABC module based on above equations is shown in Fig.5.

The sine patterns used in these equations are calculated by CORDIC module. CORDIC (COrdinate Rotation DIgital Computer) is an algorithm for computing a wide range of functions including certain trigonometric, hyperbolic, linear and logarithmic functions using simple arithmetic operations. In this paper the CORDIC algorithm version for calculating sin(ɵ) that is required in DQ-ABC block, is rotation mode of parallel CORDIC. The equations for rotation mode are:

$$x_{i+1} = x_i - y_i \cdot d_i \cdot 2^{-i} \quad (7)$$

$$y_{i+1} = y_i + x_i \cdot d_i \cdot 2^{-i} \quad (8)$$

$$z_{i+1} = z_i - d_i \cdot \tan^{-1}(2^{-i}) \quad (9)$$

Where d_i=-1 if $z_i < 0$, +1 otherwise.

Hardware implementation of parallel CORDIC consists of array of shift-add/sub stages. The maximum z_0 that can be calculated with this hardware is π/2. Therefore, a control unit is needed for $z_0 > \pi/2$ to map these angles to $z_0 < \pi/2$ range and get correct outputs. Block diagram of control unit of parallel CORDIC is shown inFig.6.

1.3.2 Three-phase hysteresis band controller

There is several pulse width modulation techniques used for various application. Some of them are sinusoidal PWM, hysteresis current controller, space vector pulse width modulation (SVPWM), etc. The hysteresis band controller provides the switching pulses for the voltage source inverter (VSI). The switching signals are determined after a comparison to the band width of the gap between the reference and the measured currents. The flowchart of this method is shown in Fig.7.

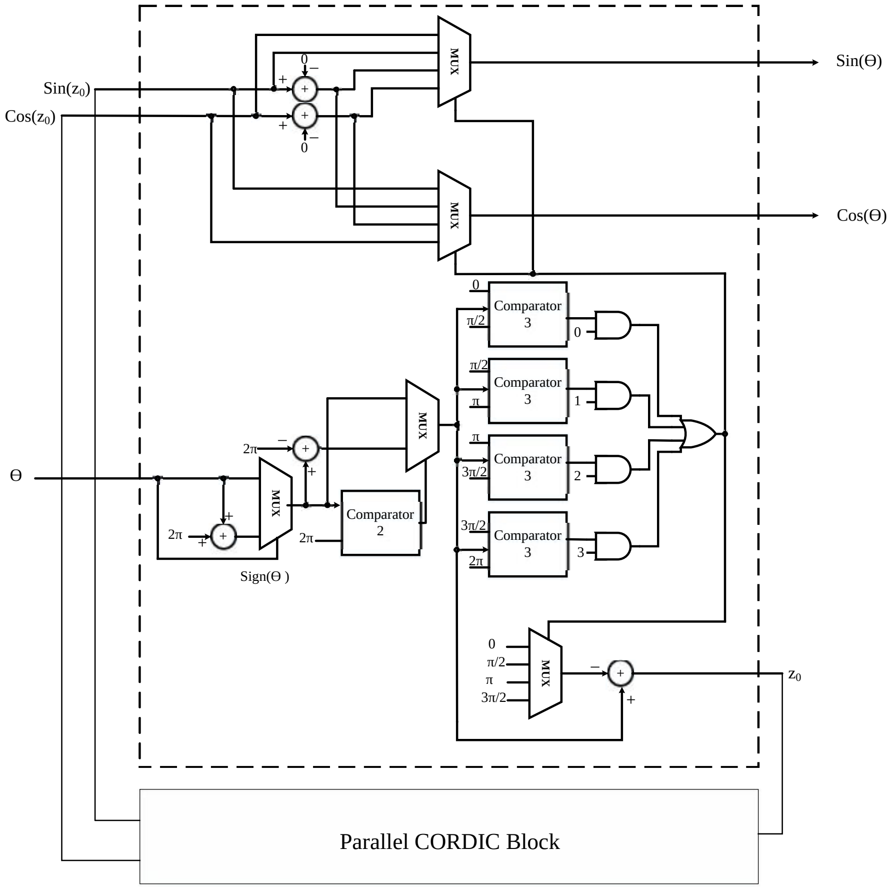


Fig.6. Block diagram of Control Unit of Parallel CORDIC

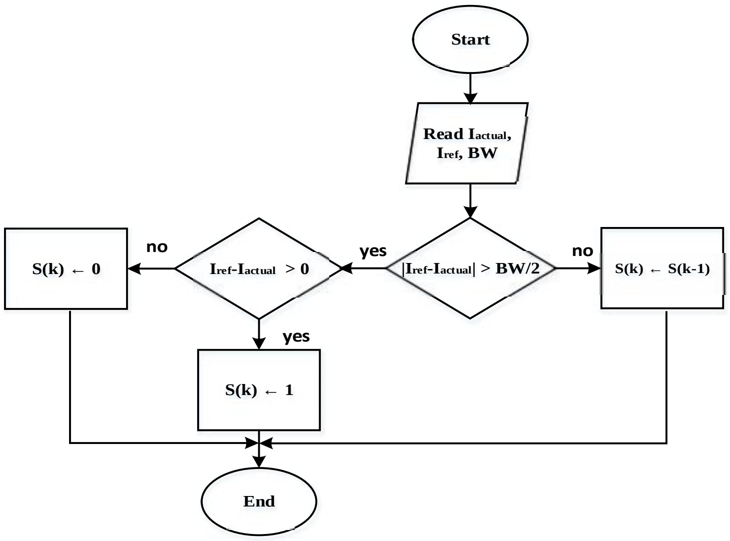


Fig.7. Flowchart of hysteresis band controller

2. RESULTS AND DISCUSSION

To validate system functionality the whole design has been simulated using MATLAB/SIMULINK. Simulation parameters are as shown in Table1. System level simulation results are shown in Fig.8 and Fig.9.

Table1. Simulation parameters

DC voltage (Udc)	550 v
Stator windings resistance (Rs)	2.875Ω
d-phase winding inductance (Ld)	8.5 e-3H
d-axis winding inductance (Ld)	805e-3H
The rotor magnetic flux (Ψ f)	0.175 Wb
Moment of inertia (J)	0.8 e-3 kg•m^2
The pole number (p)	4
Magnetic flux density (B)	0

Hardware design and implementation is carried out using Verilog HDL with 16-bit precision fixed point arithmetic. RTL simulations has been done using Modelsim software. FGPA synthesize and post-synthesize simulations are carried out using Altera Quartus II software on the Cyclone II device family. Table 2presents the time/area resources of the implemented motor controller.

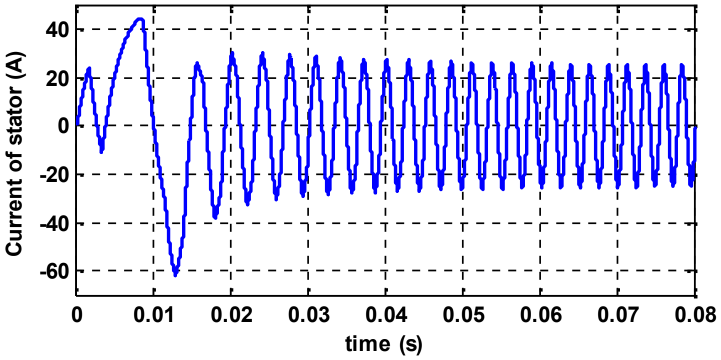


Fig.8. One of Three-phase current response curve

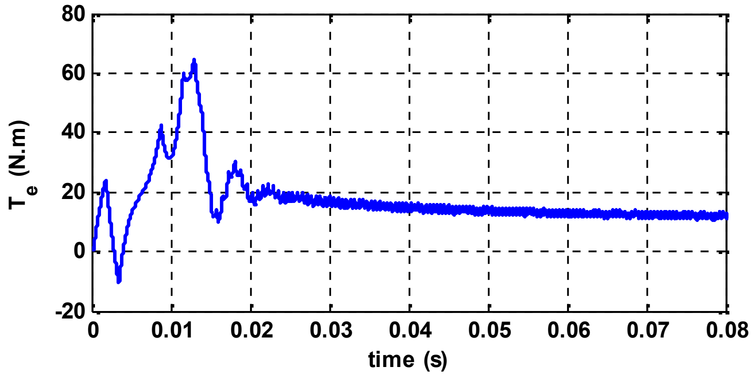


Fig.9. Electromagnetic torque waveform

Table 2. Time/Area resources

	Logic elements Precision=16 bit	% of hardware resources (over 68,416 cells)	Computation time CLK=50 MHz
Speed & position computation based on Encoder	585	0.85 %	66 ns
DQ-ABC	2280	3.33 %	330 ns
Hysteresis	96	0.14 %	60 ns
Control system based on Encoder Total	2961	4.32 %	456 ns

Fig.10 shows estimated anglular position of the rotor at 1500 rpm with proposed encoder processing unit. The simulation results in both range of high and low speed are presented in Fig.11 and Fig.12. Simulation results show that the proposed system has appropriate accuracy both in haigh and low speeds.

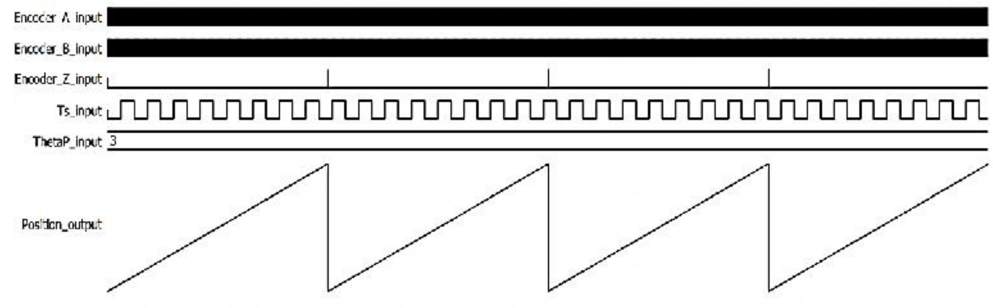


Fig.10. The simulation result of Verilog code for position computing block

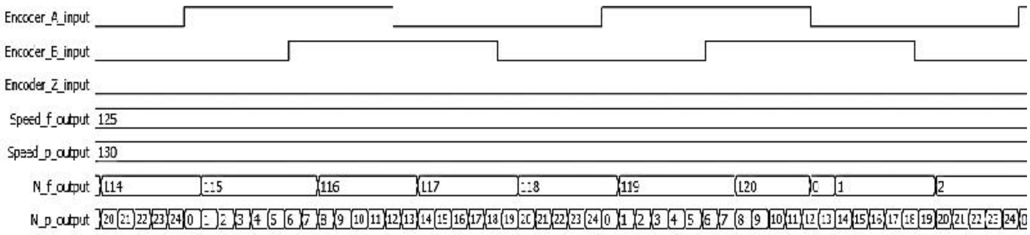


Fig.11. Simulation result of Verilog code for speed computing block in high speed range

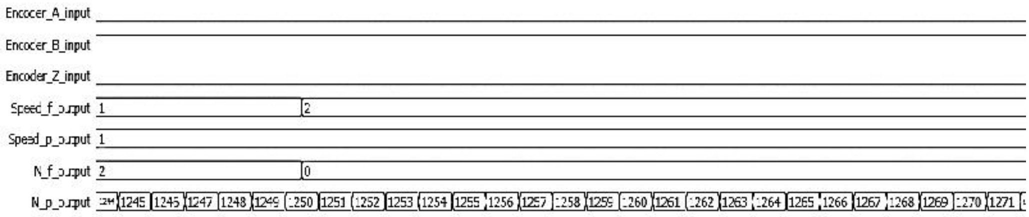


Fig.12. Simulation result of Verilog code for speed computing block in low speed range

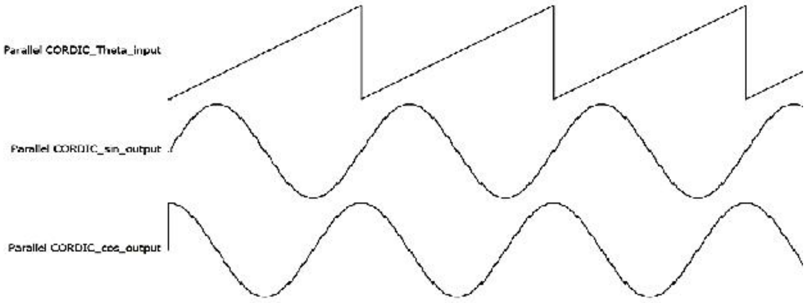


Fig.13. Simulation result of Verilog code for CORDIC block

6. REFERENCES

[1] Kung Y.-S, Tsai M.-H. FPGA-based speed control IC for PMSM drive with adaptive fuzzy control. Power Electronics, IEEE Transactions on, 2007, 22, 2476-2486

[2] Acero J, Navarro D, Barragán L, Garde I, Artigas J, and Burdío J. M. FPGA-based power measuring for induction heating appliances using sigma–delta A/D conversion. Industrial Electronics, IEEE Transactions on, 2007, 54, 1843-1852

[3] Fratta A, Griffero G, and Nieddu S. Comparative analysis among DSP and FPGA-based control capabilities in PWM power converters. Industrial Electronics Society, 2004. IECON 2004. 30th Annual Conference of IEEE, 2004, 257-262

[4] Lin-Shi X, Morel F, Llor A. M, Allard B, and Rétif J.-M. Implementation of hybrid control for motor drives. Industrial Electronics, IEEE Transactions on, 2007, 54, 1946-1952

[5] Monmasson E, Cirstea M. N. FPGA design methodology for industrial control systems—A review. Industrial Electronics, IEEE Transactions on, 2007, 54, 1824-1842

[6] Naouar M.-W, Monmasson E, Naassani A. A, Slama-Belkhodja I, and Patin N. FPGA-based current controllers for AC machine drives—A review. Industrial Electronics, IEEE Transactions on, 2007, 54, 1907-1925

[7] Rodriguez-Andina J. J, Moure M. J, and Valdes M. D. Features, design tools, and application domains of FPGAs. Industrial Electronics, IEEE Transactions on, 2007, 54, 1810-1823

[8] Ahn J.-W, Park S.-J, and Lee D.-H. Novel encoder for switching angle control of SRM. Industrial Electronics, IEEE Transactions on, 2006, 53, 848-854

[9] Van de Sype D. M, De Gussemé K, Van den Bossche A. P, and Melkebeek J. A. Duty-ratio feedforward for digitally controlled boost PFC converters. Industrial Electronics, IEEE Transactions on, 2005, 52, 108-115

[10] Kelemen Á, Imecs M. Vector Control of AC Drives. Volume 1: Vector Control of Induction Machine Drives. OMIKK-Publisher, Budapest, Hungary, 1991.

[11] Miyashita I, Ohmori Y. A new speed observer for an induction motor using the speed estimation technique. Power Electronics and Applications, 1993, Fifth European Conference on, 1993, 349-353

[12] Incze J. J, Szabó C, and Imecs M. Modeling and simulation of an incremental encoder used in electrical drives. Proceedings of 10th International Symposium of Hungarian Researchers on Computational Intelligence and Informatics, Budapest, Hungary, November, 2009, 12-14

[13] Incze I. I, Negrea A, Imecs M, and Szabó C. Incremental encoder based position and speed identification: modeling and simulation. Acta Universitatis Sapientiae, Series Electrical and Mechanical Engineering, 2010, 2, 27-39

[14] Petrella R, Tursini M, Peretti L, and Zigliotto M. Speed measurement algorithms for low-resolution incremental encoder equipped drives: a comparative analysis. Electrical Machines and Power Electronics, 2007. ACEMP'07. International Aegean Conference on, 2007, 780-787

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