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COMPARISON OF D-LATCH BASED ON CNTFET & DLATCH BASED ON MOSFET USING HSPICE

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ABSTRACT

D-Latch has applications in Memory cells and Low power D-Latchs are important for low-power digital designs. In this paper, presents design of the low power & high speed D-Latch using carbon nanotube field effect transistor (CNTFET) that utilizes different threshold voltages for best performance. In this paper, proposed design of D-Latch is simulated with HSPICE models, cmos 32nm ptm and CNTFET 32nm which Presented by Stanford University. MOSFET and CNTFET designs are simulated in different voltage & 1MHz up to 1GHz frequency and their performances are compared. The simulation result shows that the proposed D-Latch design based on CNTFET achieved an improvement in the output parameters. Finally the results of power, Delay and power delay product show that this design based on CNTFET is more optimal than its MOSFET design.

Keywords: Low power D-Latch; CNTFET; Carbon nanotubes Field effect transistors; power delay product (PDP)

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1. INTRODUCTION

The D-Latch circuit storing either a “high” or a “low” logic level when the clock pulse is low and “reading” new data from the D input when the clock pulse is high. If the data on the D input changes state while the clock pulse is high, then the output Q, follows the input D. When the CLK pulse is low, the last state of the D input is trapped and held in the latch. D latches can be used as 1-bit memory circuits or temporary buffers.

The rest of this paper is organized as follows: Section 2 describes the carbon nanotube field effect transistors. Session 3 describes the proposed design of D-Latch using CNTFET. Session 4 provide the simulation results and discussion. Session 5 provides conclusions.

2. CNTFET

Carbon nanotubes are one of the forms of carbon structures which are made of the rolled graphite sheets and they are in two types: single wall and multi wall.

Carbon Nano Tubes Field Effect Transistors (CNTFETs) have additional scalability and less scale in comparison with MOSFET transistors and this feature make them suitable for displacing of this technology [1-11].

These transistors are made of carbon nanotubes as their channel. In this paper we present a D-Latch circuit with using these features of carbon nanotubes to optimize the output parameters.

CNTFETs made by single-walled carbon nanotubes which have semiconducting properties and Single-walled carbon nanotubes formed with hollow cylinder of carbon [12]. Conductivity of nanotubes is specifying with a pair of integers that called chirality vector (m, n).Depending on the value of m and n, the nanotubes are divided into three categories: armchair, Chiral and zigzag.

Carbon nanotube field effect transistors are divided into two types of N and P.CNTFET work similar to traditional silicon transistors [13].

MOSFET-like CNTFETs are another type of CNTFETs that exhibit unipolar actions. CNTFETs has an effective feature that It will ease the designing of logic circuits and increase the performance of circuit on the other hand, the threshold voltage is related to the inverse of the nanotube’s diameter CNTFET show unique properties such as very small dimensions, very low power consumption and high speed due ballistic transport of electrons[14].

3. Proposed design of D-Latch using CNTFET:

In this paper a D-Latch circuit based on CNTFET is proposed. In this design, 18 transistors are used. Figure1 shows the proposed circuit in transistor level. This circuit has 3 inputs (D, CLK, and CLKB) and one output (Q).

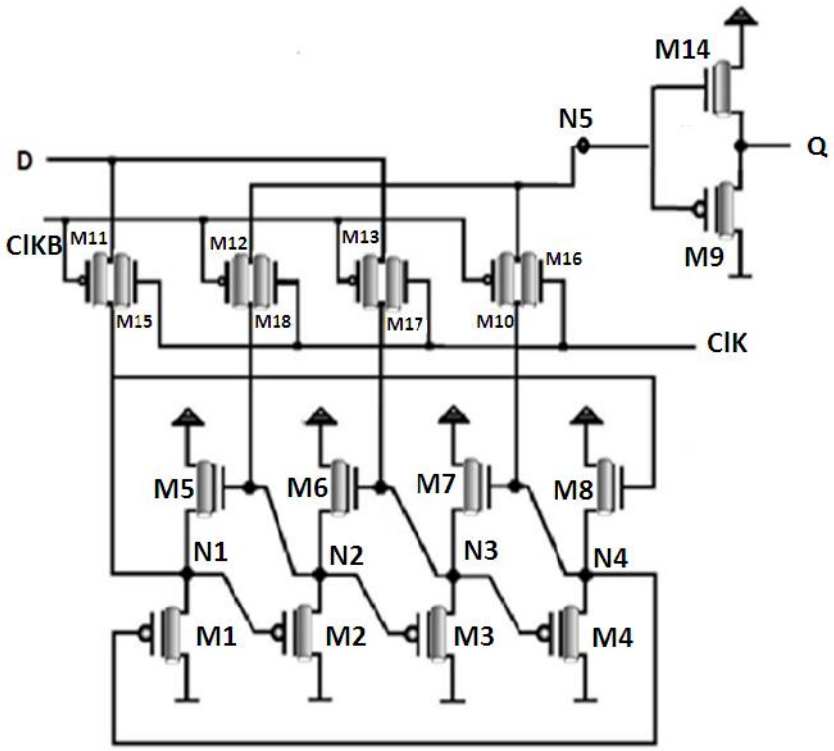


Fig.1. Proposed D-Latch Using CNTFET

Transmission gate logic is used in this design. When (CLK=1,D=1), the input switch is closed allowing new input data into the latch &both transistors of the transmission gate logic [M13,M17] are turned on and allow the signal to pass. Therefore, “1” enters & M6 will be on and we have “0” on the input of transmission gate [M12, M18], TG is turned on and passes the signal. “0” on the N5, M9 will be on and we have Q=”1”.

When (CLK=1,D=0), the input switch is closed allowing new input data into the latch &both transistors of the transmission gate logic [M11,M15] are turned on and allow the signal to pass. Therefore, “0” enters N1 & M2 will be on and we have “1” on the input of transmission gate [M12, M18], TG is turned on and passes the signal. “1” on the N5, M14 will be on and we have Q=”0”.

When CLK = 0, the input switch is opened and the output is maintained on the latest output value when clock has been 1, through feedback.

To evaluate the performance of proposed D-Latch are designed using MOSFET and CNTFET in 32nm technology. Simulations are carried out using HSPICE tool with input frequency at 1MHZ up to 1GHz [15, 16]. Transient analysis of the proposed D-Latch using CNTFET is shown in figure 2.

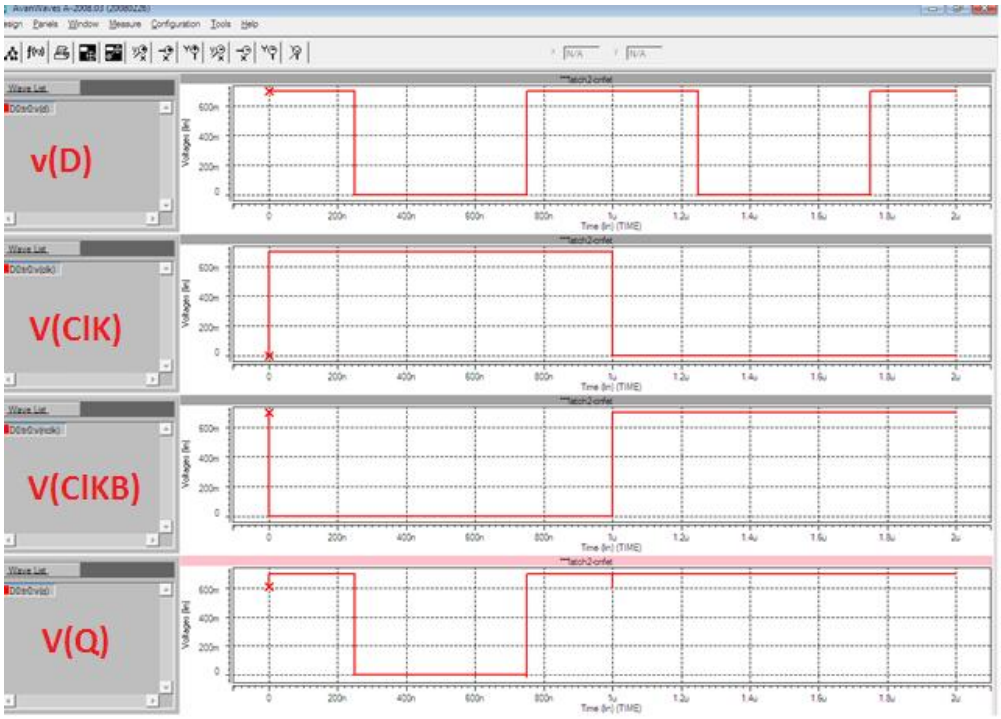


Fig.2. Transient analysis of a proposed D-Latch using CNTFET

Our first goal to use optimization methods and simulation to enhance performance of the circuit. Probable reduction of power consumption should be considered. Performance of digital circuits is studied via circuit parameters such as power consumption, delay and power delay product (PDP).

In order to study the performance of the circuit in MOSFET technology and CNTFET, delay, power consumption and PDP should be calculated and compared in different supply voltages and the clock frequency at 1MHZ up to1GHz. To calculate power dissipation, we measure the average power consumption in HSPICE.

4. SIMULATION RESULTS AND DISCUSSION

4.1 Compare Delay Variations in different frequencies of proposed D-Latch using MOSFET and CNTFET technologies

It can be seen in figure3, that delay is obtained in different frequencies and vdd=1volt. By changing the clock frequency from 1MHz up to 1GHz, delay in CNTFET circuit is about 7pS, while delay in MOSFET circuit is about 200pS. As it can be seen, by increasing the frequency in both technologies, delay does not increase with a high gradient.

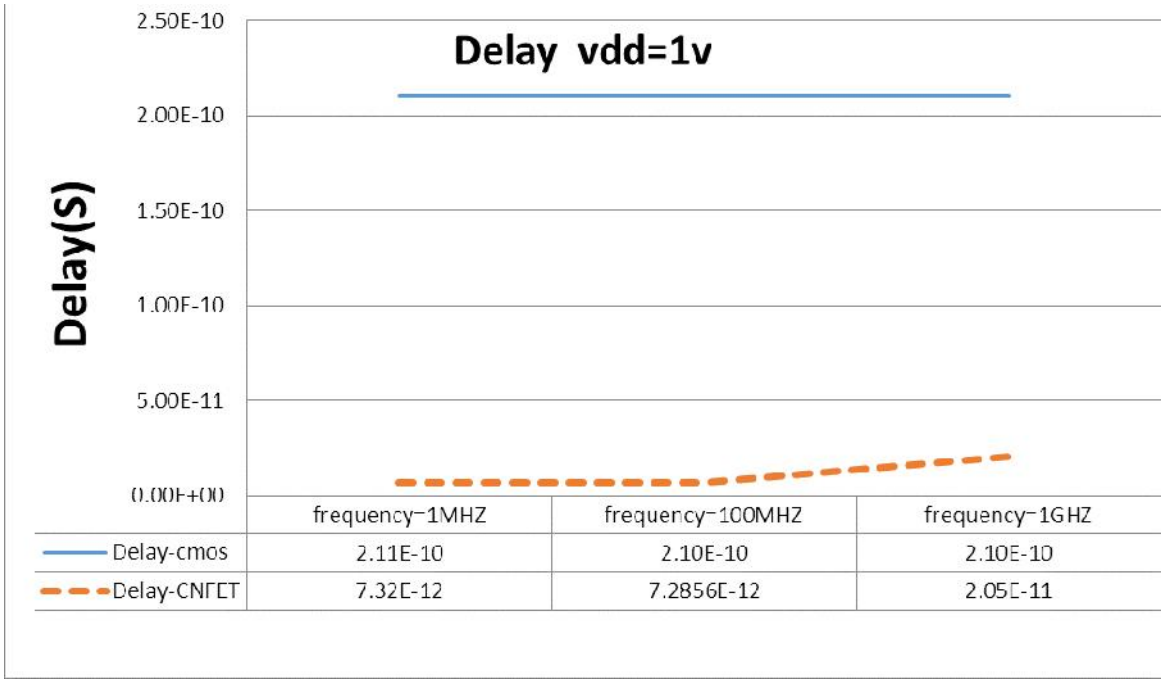


Fig.3. Delay analysis of MOSFET and CNTFET Designs

4.2 Compare Power Variations in different frequencies of the proposed D-Latch using MOSFET and CNTFET technologies

We obtain power consumption by changing frequency in circuits in both MOSFET 32nm and CNTFET 32nm technology. As it is shown in the figure 4, increasing clock frequency from 1MHz up to 1GHz, power consumption in both circuits increase. In MOSFET circuit, these variations are low but in CNTFET, these variations are large. But in all cases power consumption of CNTFET technology is much lower than MOSFET.

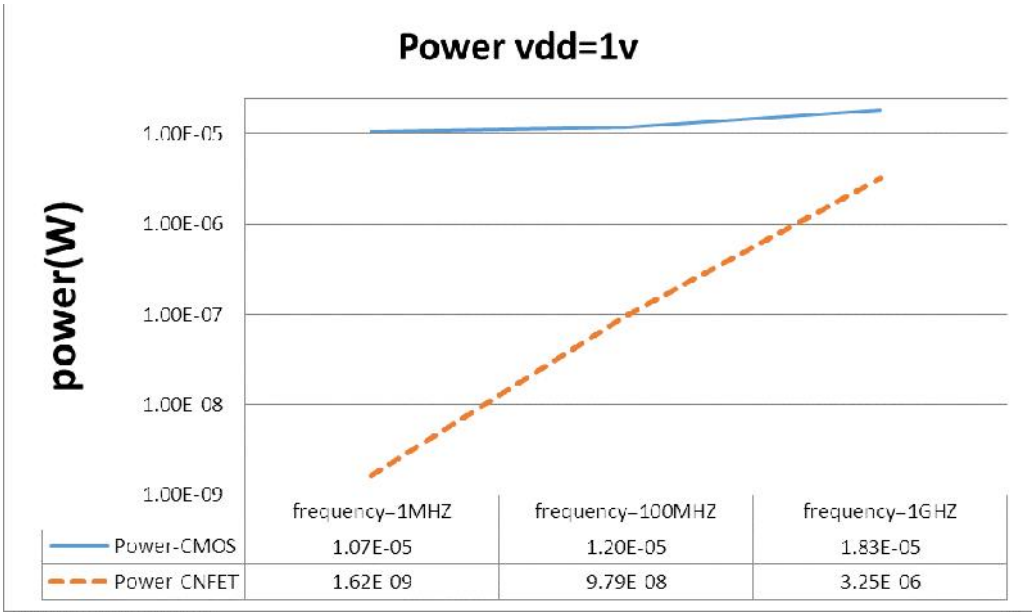


Fig.4. Average Power analysis of MOSFET and CNTFET Designs

4.3 Compare PDP Variations in different frequencies of the proposed D-Latch using MOSFET and CNTFET technologies

As shown in Figure5, by changing the clock frequency, overall performance of a circuit can be studied in 1MHz up to 1GHz frequency range. And it is observed that in all cases, PDP in CNTFET is lower than MOSFET.

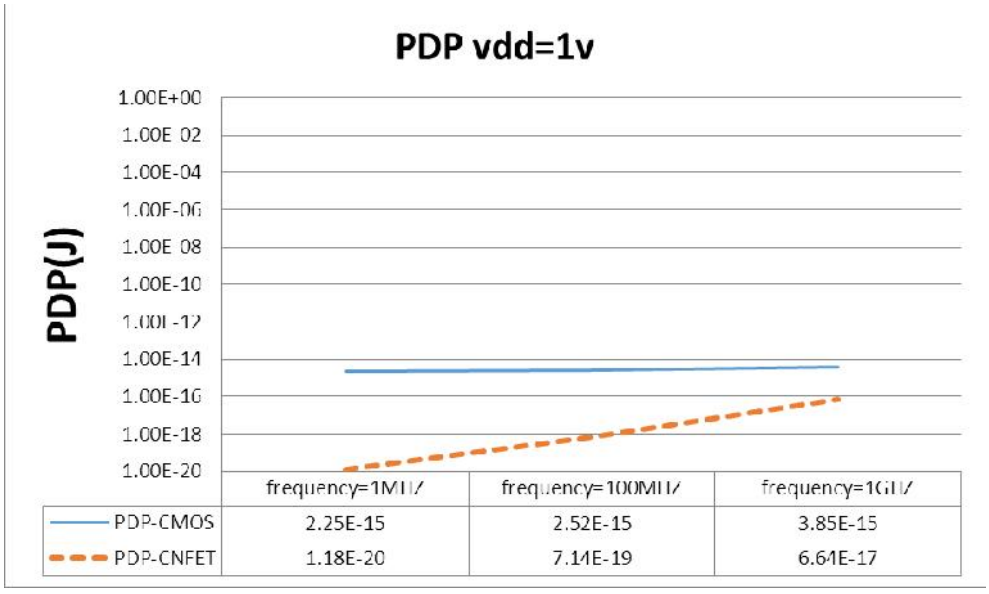


Fig.5. Power Delay Product analysis of MOSFET and CNTFET Design

4.4 Compare Delay variations of the proposed D-Latch in 100MHz and for supply voltage of (0.7 V up to 1V) in MOSFET and CNTFET technologies

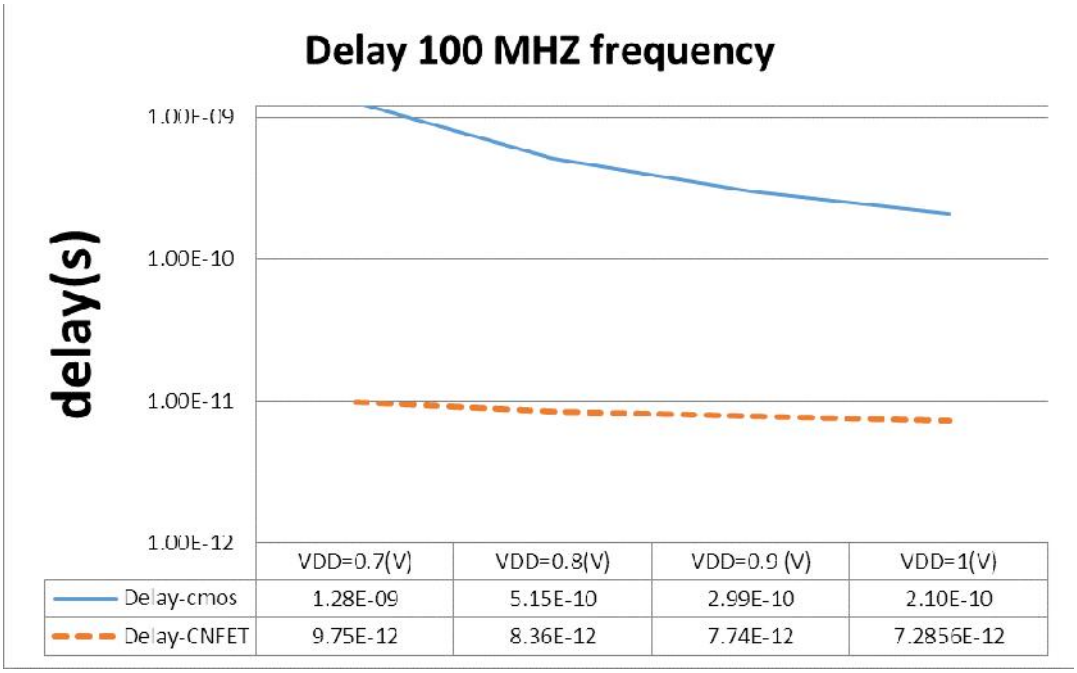


Fig.6. Delay analysis of MOSFET and CNTFET Designs

According to the diagram fig 6, as the supply voltage increases, delay is decreased and in all cases. Delay of CNTFET design is less than MOSFET in all cases. As it can be seen in this figure, changing the supply voltage in 100MHz, delay in CNTFET does not change a lot but delay variation in MOSFET is very large.

4.5 Compare Power variations of the proposed D-Latch in 100MHz and for supply voltage of (0.7-1 V) in MOSFET and CNTFET technologies

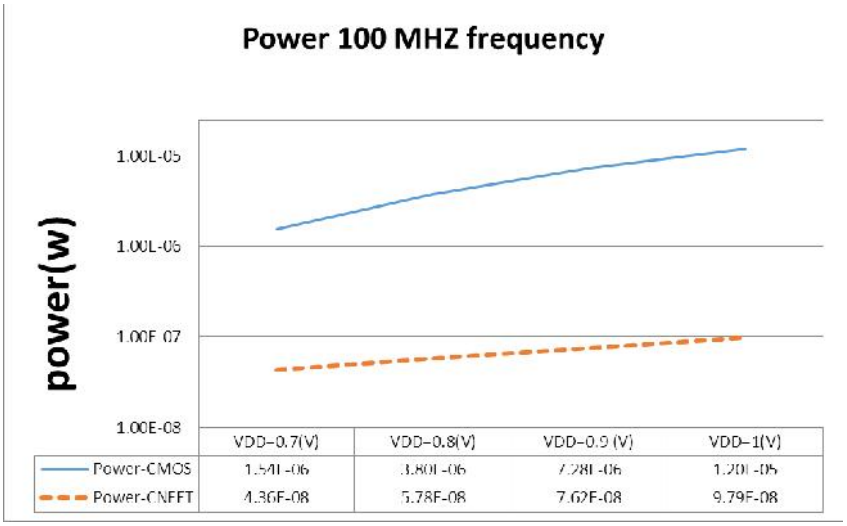
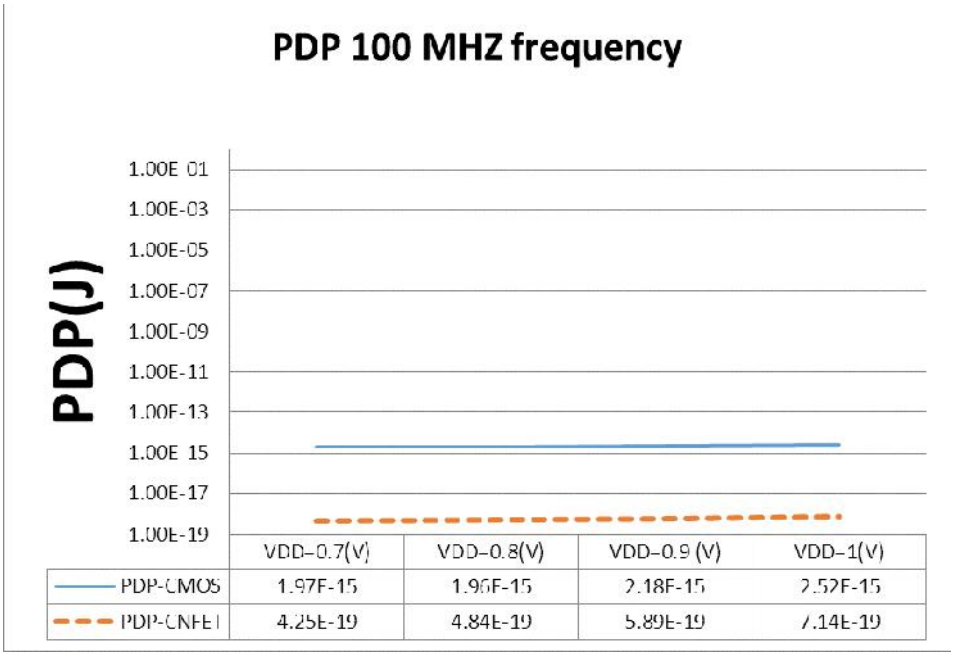


Fig.7. Average Power analysis of MOSFET and CNTFET Designs

As it can be seen in figure7, by increasing the supply voltage, power consumption is also increased. Comparing these two diagrams in different supply voltages, it is concluded that Power consumption in CNTFET technology is less than MOSFET technology. Power consumption in CNTFET is about 0.04 micro watt, while it is about 1 micro watt in MOSFET technology.

4.6 Compare PDP variations of the proposed D-Latch in 100MHz and for supply voltage of (0.7-1) volt in MOSFET and CNTFET technologies

Comparing PDP of these two circuits in MOSFET and CNTFET, it can be seen that PDP in MOSFET is very higher than PDP in CNTFET. It can be observed in the diagrams fig8 that the overall performance of the circuit in CNTFET is better than its performance in MOSFET.



	VDD=0.7(V)	VDD=0.8(V)	VDD=0.9 (V)	VDD=1(V)
PDP-CMOS	1.97E-15	1.96E-15	2.18E-15	2.52E-15
PDP-CNFET	4.25E-19	4.84E-19	5.89E-19	7.14E-19

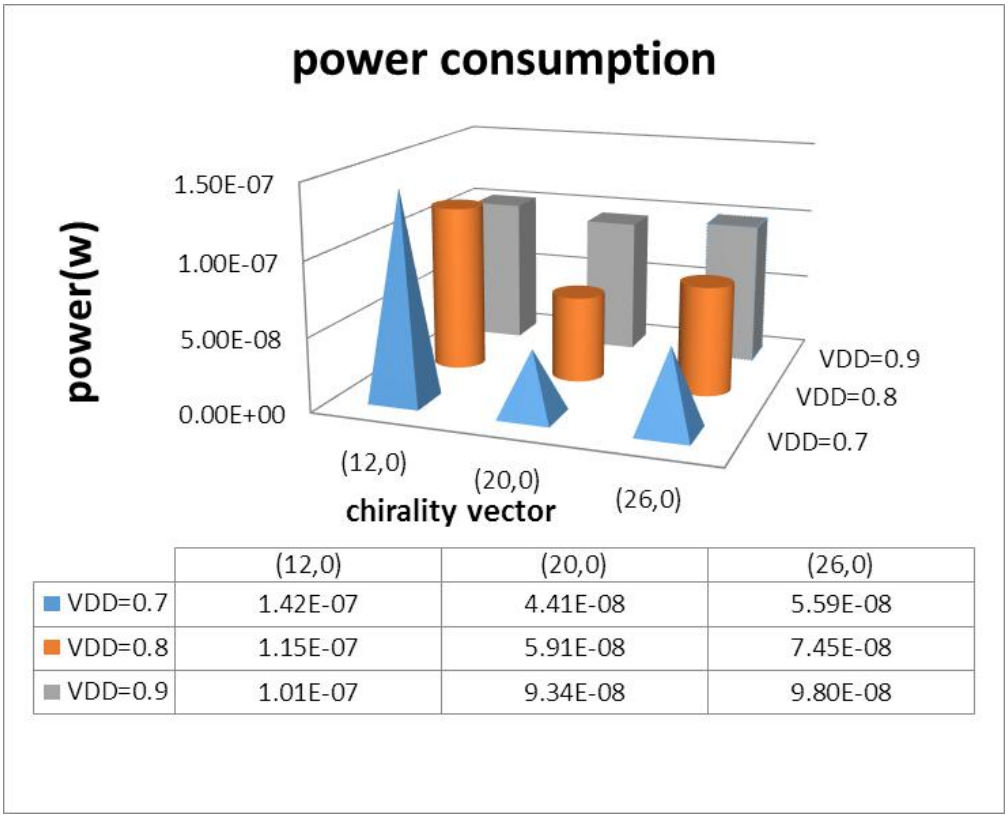
Fig.8. Power Delay Product analysis of MOSFET and CNTFET Design

4.7 enhanced performance of the CNTFET D-Latch by changing parameters of the chirality vector (n1, n2)

By changing parameters of the chirality vector and thus the threshold voltage of the CNTFET transistor, performance of the circuit is enhanced. So best chirality vector for better performance of the circuit can be found. We have simulated the circuit in CNTFET by changing parameters of the chirality vector, and in different supply voltages and in 100MHz clock frequency. Delay, power consumption and PDP are calculated.

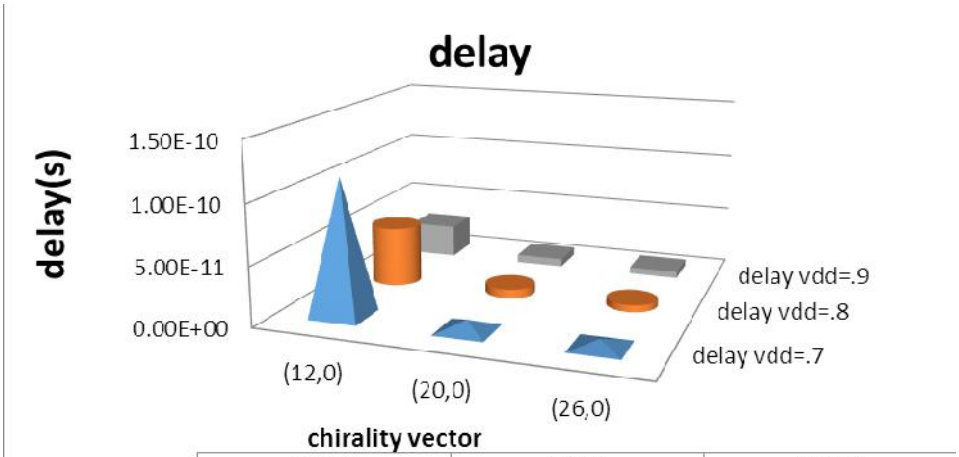
Table1. Characterizes properties of CNTFETs which are used in section

Type of transistors	Diameter of CNT	Chirality CNT	Threshold voltage	Tubes per FET
p-type	1.50894448	(19,0)	-0.2783402	3
p-type	0.95301757	(12,0)	-0.4407054	3
p-type	1.588362617	(20,0)	-0.2644232	3
p-type	2.064871403	(26,0)	-0.2034024	3
n-type	1.5089444868	(19,0)	0.2783402	3
n-type	0.9530175706	(12,0)	0.4407054	3
n-type	1.588362617	(20,0)	0.26442324	3
n-type	2.0648714031	(26,0)	0.20340249	3



	(12,0)	(20,0)	(26,0)
VDD=0.7	1.42E-07	4.41E-08	5.59E-08
VDD=0.8	1.15E-07	5.91E-08	7.45E-08
VDD=0.9	1.01E-07	9.34E-08	9.80E-08

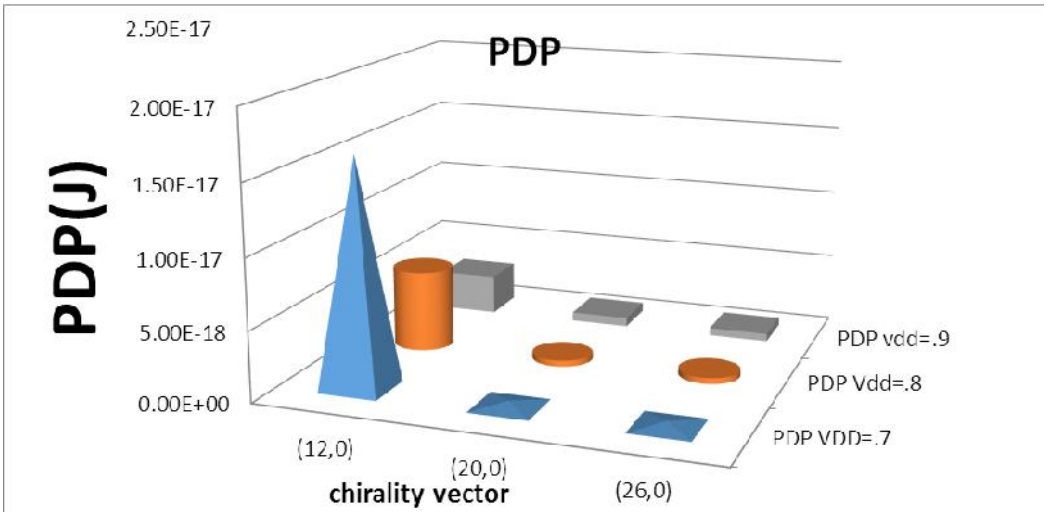
Fig.9. Power consumption variations of the proposed D-Latch in CNTFET technology by changing parameters of the chirality vector in voltages of (0.7-0.9) and clock frequency of 100MHz As it can be seen in the figure9, by changing the chirality vector in different voltages, power consumption changes and in all supply voltages it has its minimum value in chirality vector of (20, 0).



	(12,0)	(20,0)	(26,0)
delay vdd=.7	1.15E-10	8.67E-12	6.47E-12
delay vdd=.8	5.09E-11	7.52E-12	5.90E-12
delay vdd=.9	2.80E-11	6.92E-12	5.60E-12

Fig.10. Delay variations of the proposed D-Latch in CNTFET technology by changing parameters of the chirality vector in voltages of (0.7-0.9) and input frequency of 100MHz

The second parameter that is measured for evaluating the effect of chirality vector is delay. As it can be seen in the figure10. Considering the importance of this parameter and effect of molecules direction on it, it can be concluded that by increasing n1 delay is decreased. Indeed this decrease is very large near (20.0) but after this point, increasing n1 over 20, delay decreases with a mild slope.



	(12,0)	(20,0)	(26,0)
PDP VDD=.7	1.63E-17	3.83E-19	3.62E-19
PDP Vdd=.8	5.83E-18	4.44E-19	4.40E-19
PDP vdd=.9	2.84E-18	6.46E-19	5.49E-19

Fig.11. PDP variations of the proposed D-Latch in CNTFET technology by changing parameters of the chirality vector in voltages of (0.7-0.9) and input frequency of 100MHz

As it can be seen in the fig11, by increasing n1 from 12 to 20, PDP decreases and when it reaches 20, PDP reaches its minimum and by increasing n1 over 20, no tangible variation is observed in PDP of CNTFET circuit.

Table 2. Comparison result of the proposed D-Latch in CNTFET technology by changing parameters of the chirality vector in voltages of (0.7-0.9) and input frequency of 100MHz

PDP	**Vdd=.7**	**Vdd=.8**	**Vdd=.9**
(12,0)	1.63E-17	5.83E-18	2.84E-18
(20,0)	3.83E-19	4.44E-19	6.46E-19
(26,0)	3.62E-19	4.40E-19	5.49E-19
DELAY	**Vdd=.7**	**Vdd=.8**	**Vdd=.9**
(12,0)	1.15E-10	5.09E-11	2.80E-11
(20,0)	8.67E-12	7.52E-12	6.92E-12
(26,0)	6.47E-12	5.90E-12	5.60E-12
POWER	**Vdd=.7**	**Vdd=.8**	**Vdd=.9**
(12,0)	1.42E-07	1.15E-07	1.01E-07
(20,0)	4.41E-08	5.91E-08	9.34E-08
(26,0)	5.59E-08	7.45E-08	9.80E-08

4.8 The Reliability of Performance proposed D-Latch circuits based on CNTFET & MOSFET in different supply voltages & frequency

Simulation results show CNTFET D-Latch circuit is significantly enhanced optimization in terms of circuit parameters & more reliable. But the D-Latch circuit based on 32nm MOSFET does not work well in 100MHz frequency and 1GHz frequency & supply voltage of 0.4 -0.7 volt that failed output waveform in 0.7V in MOSFET technology shown in fig 12.

Table 3. Circuit parameters in different supply voltage& 1GHZ frequency

POWER GHZ	vdd=0.4	vdd=0.7	vdd=1
cmos 32nm	failed	failed	1.83E-05
CNTFET 32nm	2.05E-07	1.15E-05	3.25E-06
DElAY GHZ	vdd=0.4	vdd=0.7	vdd=1
cmos 32nm	failed	failed	2.10E-10
CNTFET 32nm	4.53E-11	1.35E-10	2.05E-11
PDP GHZ	vdd=0.4	vdd=0.7	vdd=1
cmos 32nm	failed	failed	3.85E-15
CNTFET 32nm	9.28E-18	1.55E-15	6.64E-17

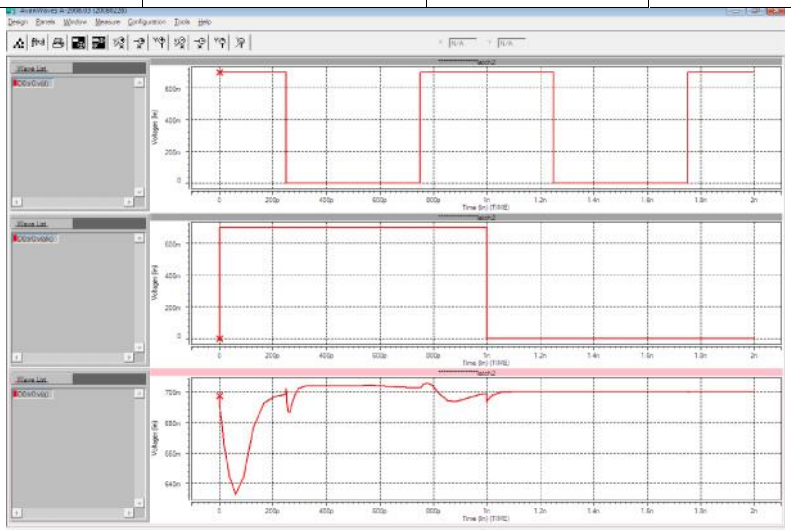


Fig.12. Failed output waveform in 0.7V& 1GHZ frequency in MOSFET technology

4.9 Comparison proposed design with the previous work presented in [17]

Table 4. Comparison of the proposed D-latch based on CNTFET with the other CNTFET D-latch in vdd=0.8(v) presented in [17]

Parameter	design 1	design 2	design 3	proposed design
PDP	2.13E-18	1.54E-17	1.21E-18	9.11E-21
DELAY	1.54E-12	1.17E-11	7.53E-13	8.36E-12
POWER	1.38E-06	1.31E-06	1.60E-06	1.09E-09
Number of Transistor	10	8	4	18

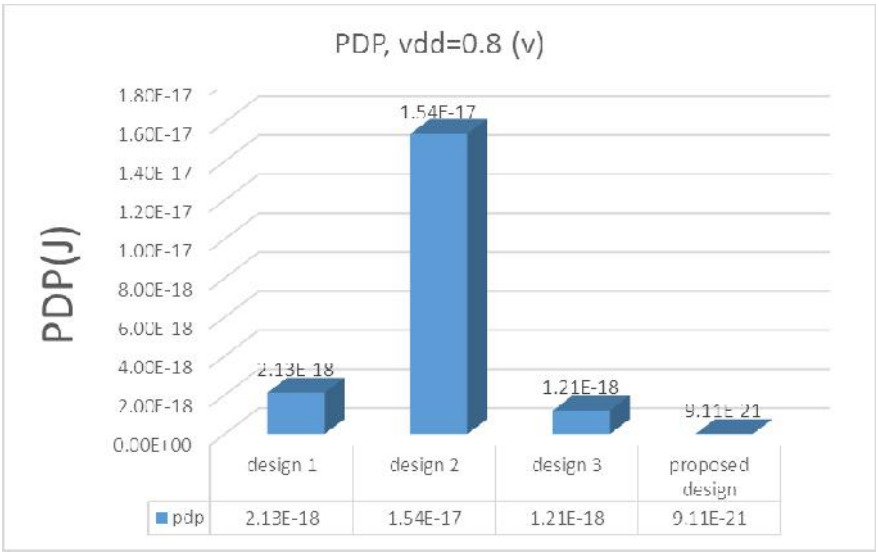


Fig.13. PDP Comparison of the proposed circuit based on CNTFET with the other CNTFET D-latch presented in [17]

Considering the obtained power consumption, delay and PDP through simulation, and with compare the other D-Latch circuit presented in [17] & they are shown in fig 13, table4, it can be said that proposed D-Latch circuit based on CNTFET are more optimal than the other D-Latch circuits presented in [17].

5. CONCLUSIONS

In this paper, we presented designs of D-Latch based on CNTFET, the proposed D-Latch is simulated in HSPICE 32nm MOSFET and 32nm CNTFET technologies, in different supply voltage of 0.4V to 1V and clock frequency at 1MHZ up to1GHz in MOSFET and CNTFET designs.

The simulations show that by using carbon nanotube field effect transistors we have achieved a significant improvement in delay, power and power delay product. The results in different threshold voltages leads in that have the best performance in our circuit design. Hence the proposed D-Latch using CNTFET is more efficient for low power and high performance applications.

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