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Level shifter for low power applications with body bias technique

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Abstract

In present work three new designs of level shifter in 0.35µm technology using body bias approach have been presented. The level shifters, namely conventional type-I, conventional type-II and contention mitigated have been improved by varying the reverse body bias from 0.1V to 0.5 V. Circuits have been simulated in Spice with TSMC0.35 process technology. Output level of 3.3V has been obtained with input pulse of 1.6V. Modified conventional type-I level shifter shows minimum power consumption of 90.1250pW as compared to 498.33pW for conventional type-I. Further, modified conventional type-II gives minimum power of 480.28pW as compared to 3479pW with existing circuit. Third proposed circuit namely modified contention mitigated level shifter (CMLS) show minimum power consumption of 85.52pW as compared to 493.73pW for circuit without modifications. Simulation results show that proposed circuits are able to shift 1.6V to 3.3V with reduced power consumption with little conciliation in delay.

Keywords: Body bias, CMOS, level shifter, leakage current and power consumption.

1. Introduction

With the rapid growth in high speed computation and battery operated devices like laptops, palmtops, personnel note books etc., power conservation has become major design concern for very large scale integration (VLSI) circuits and system design (Leblebici and Kang, 1998). It is also becoming a major concern for deep submicron (DSM) technologies. The shrinkage in size and addition of more function on integrated circuits(IC) has given rise to large power dissipation per unit area thereby increasing the packaging and cooling costs. Reliability problems also arise with increase in power consumption (Liqiong *et al.*, 2000). Other design consideration for integrated circuits includes size, propagation delay, throughput and cost of portable systems. Power consumption in VLSI circuit includes dynamic, static power and leakage power consumption (Sedra and Smith, 1998; Roy and Prasad, 2002). Dynamic power consumption results from switching of load capacitance between two different voltages and dependent on frequency of operation (Chandrakasan *et al.*, 1992). Whereas static power is contributed by direct path short circuits currents between supply (VDD) and ground (VSS). Leakage power results from leakage currents that arise from substrate injection and sub-threshold. Leakage power depends on the total number of transistors and their operating condition in spite of their switching activity. Power consumption can be reduced by scaling supply voltage and capacitance (Roy and Prasad, 2002). Problems of small voltage swing, insufficient noise margin and leakage currents start to originate with the scaling the power supply voltage. Other methods for power saving include body biasing, power down strategies, minimization of effective switching capacitances etc. (Bero *et al.*, 2006; Hamada *et al*, 2008; Ekekwe *et al.*, 2006; Imai *et al.*, 2005; Zhai *et al.*, 2004).

Level shifters are the core elements in various electronic systems and these are used to convert the logic signal from one voltage level to other. These are also important circuit component in multi voltage systems and have been used between core circuits and I/O circuit of integrated circuits. In recent years multi core processors supply voltage scaling technique has been used in non critical components for reduced power consumption (Zhang, *et al.*, 2006; Hattori, *et al.*, 2006). This results in a condition where different blocks of System on Chip (SoC) design operate at different supply voltages for minimum energy consumption. Therefore voltage level shifters are crucial circuit component for interfacing blocks with different supply voltages. A variety of level shifter

designs have been reported in literature with single and dual supply voltage schemes (Kkmeno *et al*, 2000; Wooters *et al*, 2010; Liu *et al.*, 2010; Chan *et al.*, 2005; Jeong *et al.*, 2008). Conventional level shifter (Type-I and Type-II) with low voltage supply VddL and high voltage supply VddH has been reported (Chavan *et al.*, 2008; Koo *et al.*, 2005; Zhang *et al.*, 2006). The conventional level shifter have disadvantage of large power consumption, delay variation due to different current driving capabilities of transistors and malfunctioning at low supply core voltage VddL (Zhai *et al.*, 2004). Level shifters with bootstrapping technique are reported in (Garcıa-Montesdeoca *et al*, 2009;. Tan *et al*, 2002). Contention mitigated level shifter (CMLS) with reduced power consumption as compared to conventional shifters are also reported (Chan *et al.*, 2005). Capacitive coupling type level shifter using low temperature poly-Si (LTPS) with reduced power consumption has also been reported (Eun-Jeong *et al.*, 2008).

With the continuous increase in operating frequency and number of level converters in integrated circuits, power consumption has become significant design issue. Improvement in power consumption of level shifter affects the total power consumption of any VLSI system. Due to quadratic effect of supply voltage, power consumption can be reduced by scaling supply voltage but circuit performance is also degraded in terms of delay, noise margin etc. (Chandrakasan *et al*, 1992; Roy and Prasad 2002). Alternative scheme need be employed for reduction in power consumption so that system performance is not degraded. To reduce the standby leakage in CMOS circuits, a reverse body biasing is usually used. Body biasing techniques make use of body terminal bias as another control mechanism to dynamically tune threshold voltages. Threshold voltage (Vth) is related by the square root of the bias voltage implying that a significant voltage level would be needed to raise the Vth. By application of reverse body bias, the Vth is increased as given in equation (1), which subsequently reduces the sub threshold leakage currents (Sedra and Smith 1998; Roy and Prasad 2002). By controlling Substrate bias voltage (V_{sb}) leakage current are minimized and hence power consumption is reduced.

$$V_t = V_{t0} + \gamma\left(\sqrt{2\phi_f + V_{sb}} - \sqrt{2\phi_f}\right) \quad (1)$$

Where V_{t0} is threshold voltage for $V_{sb} = 0V$; ϕ_f is Fermi potential and γ is substrate bias coefficient.

In the current work, modifications have been proposed in existing circuits using reverse body bias technique. Modified circuits show reduced power consumption with adequate performance levels. The rest of paper is organized as follows: in Section II body biasing has been applied to existing circuits and modified circuits have been presented. In Section III the results of modified circuits have been presented and compared with existing circuits. Conclusions have been presented in Section IV.

2. System Description

For improvement in power consumption of CMOS level shifter namely conventional type-I, conventional type-II and contention mitigated, reverse body biasing technique has been applied. Gate length of NMOS & PMOS transistors have been taken as 0.35µm. Width of NMOS & PMOS transistors have been taken as 1.0 and 2.5µm respectively. Supply voltage VddH and VddL are taken as 3.3V & 2.2V respectively. Input pulse of 1.6V with 100 MHz frequency has been taken for all circuits.

Modified conventional type-I level shifter using body bias techniques with additional voltage source V1 is shown in Figure 1. PMOS transistors [P1-P3] have been biased to VddH and transistors P4 & P5 have been biased to VddL. NMOS transistors [N1-N5] have been biased to V1 [0.1-0.5] V instead of ground.

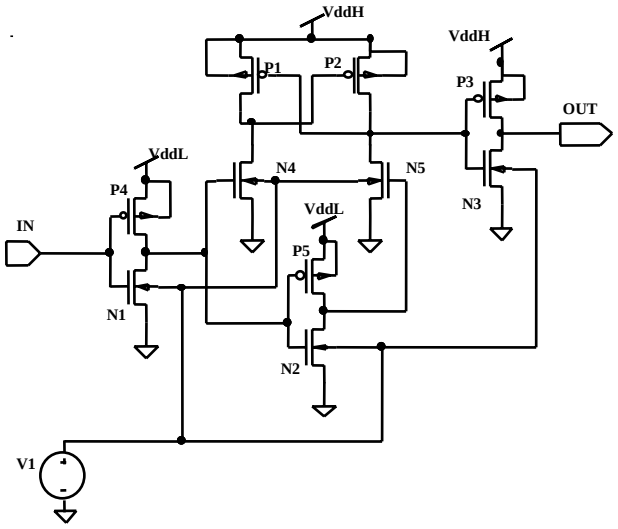

Figure 1. Conventional type-I level shifter with body bias

Figure 2 shows modified conventional type-II level shifter with reverse body biasing. PMOS transistors P1&P2 have been biased to VddH and transistor P3 has been biased to VddL. NMOS transistors [N1-N3] have been biased to V1 [0.1-0.5] V.

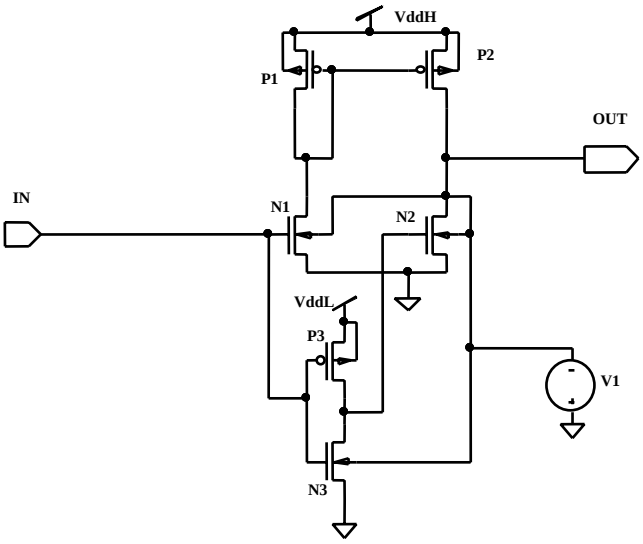

Figure 2. Conventional type-II level shifter with body bias

Figure 3 show contention mitigated level shifter (CMLS) with reverse body biasing. PMOS transistors [P1-P5] have been biased to VddH and transistors P6&P7 have been biased to VddL. Body terminal of NMOS transistors [N1-N5] have been biased to V1 [0.1-0.5] V.

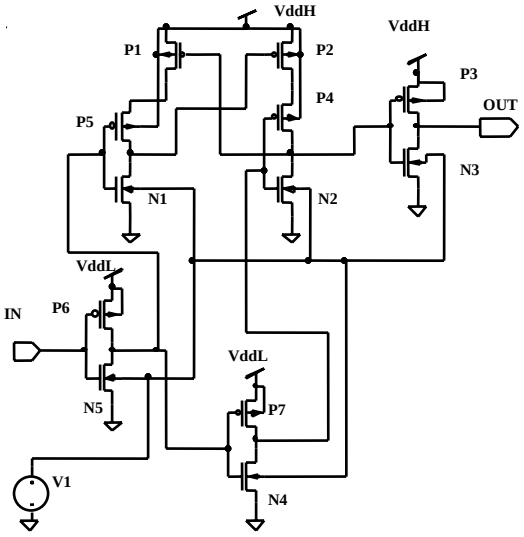

Figure 3. Contention mitigated level shifter with body bias

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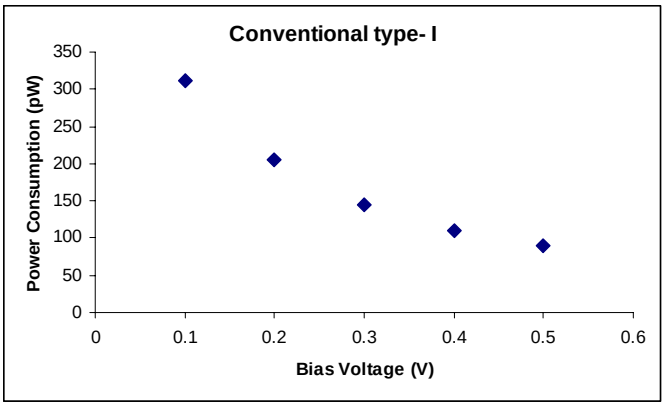
3. Results and Discussions

Proposed and existing level shifter circuits have been simulated in 0.35µm technology using TSMC 0.35 model file with same set of input parameters and comparisons have been made. Table 1 show the results of power consumption and delay for modified level shifter designs with varied bias voltage from [0.1-0.5] V. Modified conventional level shifter type-I show minimum power dissipation of 90.12pW and delay of 5.3724ns at reverse body bias of 0.5V. Further, conventional type-II level shifter circuit's gives minimum power dissipation of 480.28pW and delay of 0.1226488ns with 0.5V body bias. Moreover, modified contention mitigated level shifter shows minimum power dissipation of 85.52pW and delay of 0.427580ns with 0.5V body bias. Figure 4 (a)

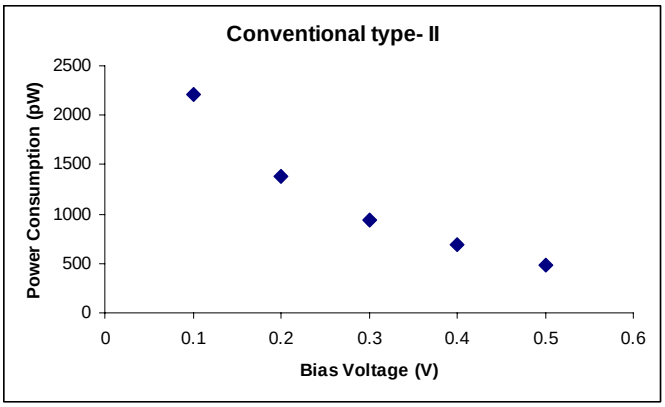
(b) and (c) shows power consumption variations of three modified level shifters with varied reverse bias voltage from 0.1V to 0.5V. Figure 5(a),(b),(c)show delay variation of modified circuits with varied reverse bias voltage from 0.1V to 0.5V. It has been observed from results that power consumption reduces considerably with increase in reverse bias. It has also been observed that there is little increase in delay with increase in reverse bias voltage. Figure (6) shows input and output waveform of modified level shifter at bias voltage of 0.2V.

Table 1. Results of proposed level shifter circuits

Bias Voltage (V)	Level shifter configurations					
	Modified conventional type-I level shifter		Modified conventional type-II level shifter		Modified contention mitigated level shifter	
	Power Consumption (pW)	Delay (ns)	Power Consumption (pW)	Delay (ns)	Power Consumption (pW)	Delay (ns)
0.1	310.7590	2.7514	2209.7	0.112088	306.1605	0.3982240
0.2	205.6850	3.2149	1377.2	0.1148531	201.0865	0.4048899
0.3	145.4804	3.6813	939.3620	0.1175174	140.8819	0.4117934
0.4	110.4990	4.4685	687.7304	0.1200811	105.9005	0.4198419
0.5	90.1250	5.3724	480.2857	0.1226488	85.5265	0.427580

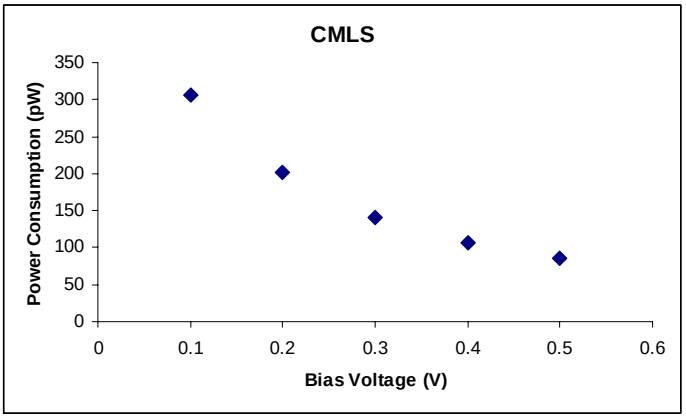


(a)



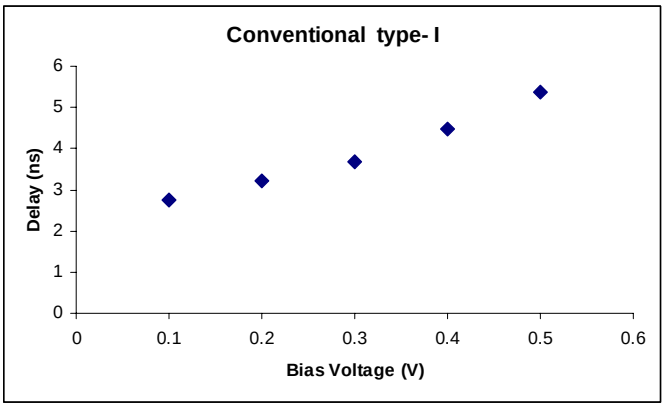
(b)

Figure 4. Power consumption with reverse bias (a) Conventional Type-I (b) Conventional Type-II

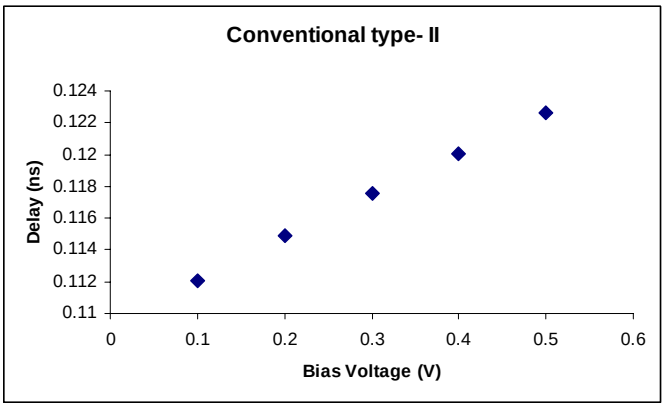


(c)

Figure 4. Power consumption with reverse bias (c) CMLS level shifter

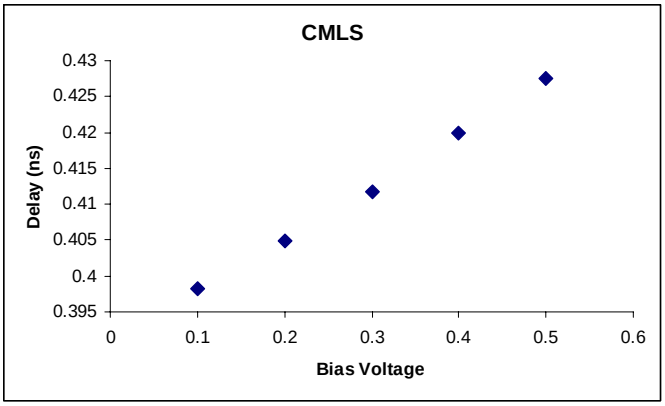


(a)



(b)

Figure 5. Delay variation with reverse bias (a) Conventional Type-I (b) Conventional Type-II



(c)

Figure 5. Delay variation with reverse bias (c) CMLS level shifter

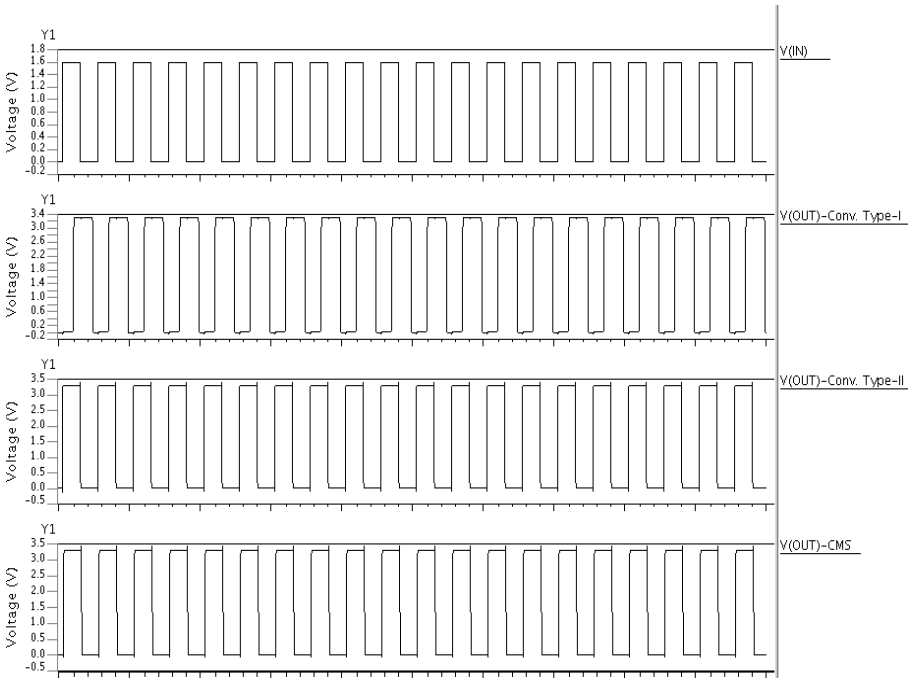


Figure 6. Input and output waveform of modified level shifter at 0.2V reverse bias

Table 2 shows results of power dissipation and delay for existing level shifter circuits. Conventional level shifter type-I gives power dissipation of 498.33pW with delay of 2.2744ns whereas conventional type-II dissipates 3479pW with 0.10925ns. CMLS shows power dissipation of 493.73pW with delay of 0.391815ns.

Table 2. Results for existing level shifters without body bias

Level shifter configurations	Power Consumption(pW)	Delay(ns)
Conventional type-I level shifter	498.33	2.2744
Conventional type-II level shifter	3479	0.10925
Contention mitigated level shifter	493.73	0.391815

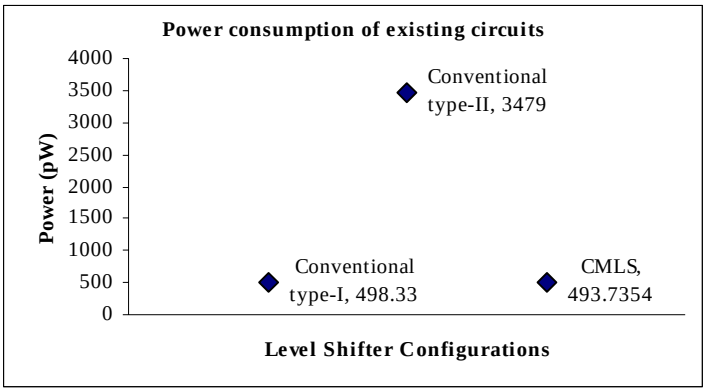


Figure 7. Power consumption of existing level shifter circuits

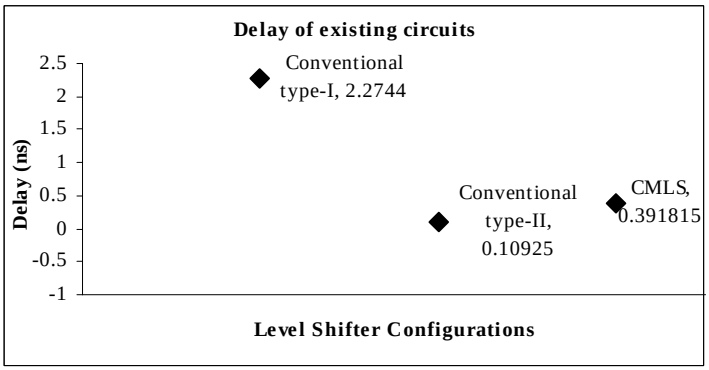


Figure 8. Delay of existing level shifter circuits

Figure.7 and 8 shows power consumption and delay results for level shifter circuits without reverse body bias. It has been observed from comparisons of Table 1 and Table 2 that power consumption has been reduced with proposed circuits with a little conciliation in delay. It has also been observed that power consumption does not reduce monotonically with increase in reverse bias and dependent on leakage currents components. Optimum body bias is a characteristic of process technology where minimum leakage current takes place. Reverse body bias approach is better than bootstrapped technique and level shifter with LTPS as extra capacitance is added for reduction in power consumption which subsequently increases the delay in circuits. Reverse body bias approach is also superior to cluster voltage scaling and variable supply voltage as additional hardware and complexity is also added in these techniques, which further increases chip area to the system. Present approach reduces the power consumption with minimum circuit complexity and with little compromise in delay.

4. Conclusions

In reported work, three circuits, modified conventional type-I, type-II and modified CMLS using reverse body bias technique have been presented. Bias voltage has been varied from [0.1-0.5] V. Results of power consumption and delay have been obtained and compared with previously reported circuits. Modified conventional type-I level shifter show minimum power consumption of 90.1250pW as compared to 0.49833nW for conventional type-I. Second proposed circuit conventional type-II gives minimum power of 480.28pW compared to 3479pW with existing circuit. Third proposed circuit namely modified CMLS shows minimum power consumption of 85.52pW as compared to 0.4937354nW for circuit without modifications. Maximum output delay results also have been obtained for proposed circuits and it has been observed that with little concession in delay, power consumption has reduced significantly with the proposed method.

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