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International Journal of Engineering, Science and Technology
Vol. 14, No. 3, 2022, pp. 85-93

INTERNATIONAL JOURNAL OF ENGINEERING, SCIENCE AND TECHNOLOGY

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A seven-level cascaded multilevel inverter based on simplified SVPWM method

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Abstract

The multilevel converters are extremely widespread alternatives within megawatt power level as well as medium voltage level applications due to their excellent execution than the typical two-level converters. The widely applied control strategies aimed at inverters are Sine Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) strategies. In between these two PWM methods, the SVPWM strategy has excellent execution as compared to the SPWM strategy as a result of improved DC link voltage use as well as a decrease in Total Harmonic Distortion (THD) in output voltages. A traditional SVPWM strategy owns numerous weaknesses like computational complications in terms of identification of the reference voltage vector position, to identify sector, triangle and also it requires large memory for storing look up tables used for switching vectors. This paper presents, an innovative modified SVPWM strategy aimed at Cascaded H-Bridge Multilevel Inverter (CHBMLI). The novel modified SVPWM strategy has overwhelm the downsides of traditional SVPWM strategy. A seven-level CHBMLI is used for the implementation of this simplified SVPWM method to assess performance and as well to made comparison with the SPWM strategy. A MATLAB software is used for the simulation.

Keywords: SVPWM, SPWM, Simplified SVPWM, CHBMLI.

DOI: http://dx.doi.org/10.4314/ijest.v14i3.10S

Cite this article as:

Matale N.P., Thakre M.P., Borse P.S. 2022. A seven-level cascaded multilevel inverter based on simplified svpwm method, *International Journal of Engineering, Science and Technology*, Vol. 14, No. 3, pp. 85-93. doi: 10.4314/ijest.v14i3.10S

Received: January 14, 2022; Accepted: January 14, 2022; Final acceptance in revised form: January 17, 2022

This paper was earlier presented at the SDCEE-2021: 1st International Online Conference on Sustainable Development in Civil and Electrical Engineering, National Institute of Technology Kurukshetra, Kurukshetra, India, December 17-19, 2021 and substantially improved for this Special Issue. Guest Editors: (i) Dr. Sri Niwas Singh, Professor (HAG), Department of Electrical Engineering, Indian Institute of Technology Kanpur, 208016 (U.P.) India, Director, ABV-Indian Institute of Information Technology & Management Gwalior; (ii) Dr. Ashwani Kumar, SMIEEE, Fellow IE (I), Fellow IETE (I), LMISTE, LMSCIEI, Professor and Head, Department of Electrical Engineering, NIT Kurukshetra Haryana, India. Dr. Kumar has 27 years teaching experience and an industrial experience of 2 years, 8 months.

1. Introduction

The necessity of megawatt power and medium voltage level rating equipments within numerous manufacturing processes has been enlarged considerably in the past few years (Rodriguez *et al*, 2009). The large number of motor drives used in various manufacturing processes need megawatt power along with medium voltage level for their satisfactory operation. For such applications, the best option is multilevel inverters (Kouro *et al*, 2010). A staircase waveform of voltage is produced by the multilevel inverter using DC voltage sources and semiconductor switches. The main advantages of multilevel inverters in

comparison with the two-level inverter are drop in harmonics of line voltages and output currents, fewer voltage stress across semiconductor switches, a lesser amount of common mode voltage and improved output wave shape quality (Rodriguez *et al*, 2002). A CHBMLI, Flying-Capacitor (FCMLI) and Diode-Clamped (DCMLI) are the three topologies of multilevel inverter. The CHBMLI is highly popular than other topologies of multilevel inverter due to its merits like extremely integrated construction and less quantity of devices like diodes and capacitors as required in the other two topologies (Rodriguez *et al*, 2007; Maurya *et al*, 2020).

A modulation method plays vital role in the working of all these multilevel inverters. The widely used modulation methods for inverters are SPWM and SVPWM (Attique *et al*, 2017). A SPWM method based on Phase Disposition (PD) is generally used aimed at multilevel inverters because of its merits such as easy execution and lesser computational problem (Sanjay *et al*, 2018). As an alternative, a SVPWM strategy is beneficial as compared to a SPWM strategy owing to improved DC link voltage use, reduced harmonics along with able to operate within over-modulation range (Chowdhary *et al*, 2020; Srivastava *et al*, 2020; Thakre *et al*, 2021; Hu *et al*, 2007; Thakre *et al*, 2020). A conventional SVPWM strategy needs large number of operating stages such as identification of sector number on the basis of reference voltage vector position, finding number of triangles along with its type, calculation of ON periods of dynamic vectors after that the choice of redundant switching conditions, generation of switching order and finally to calculate the ON periods designed for every semiconductor switch (Thakre *et al*, 2020; Manasa *et al*, 2011; Rushiraj *et al*, 2016; Thakre *et al*, 2020).

An implementation of the conventional SVPWM method is comparatively hard due to a large number of triangles plus the large number of surplus switch conditions existing inside the Space Vector Diagram (SVD) (Sabarad *et al*, 2015; Ray *et al*, 2019; Ibrahim *et al*, 2014). In (Prasad *et al*, 2017; Beig *et al*, 2007; Seo *et al*, 2001; Mohamed *et al*, 2009; Ahmed *et al*, 2016), the technique is presented on the basis of disintegrating a three-level SVD into six two-level SVD resulting into large difficulties for higher voltage levels. An additional SVPWM procedure is stated in (Wu et al, 2020; Celanovic *et al*, 2001; Gupta *et al*, 2006) on the basis of 60-degree co-ordinate system has weaknesses such as inappropriate switching conditions and voltage unevenness difficulties within a capacitor. In this paper, an innovative simplified SVPWM strategy aimed at a seven-level CHBMLI is presented. This new simplified SVPWM strategy does not want sector identification, lookup tables and computations as needed within traditional SVPWM strategy.

2. Cascaded H-Bridge Multilevel Inverter

A CHBMLI is widely used topology of the multilevel inverter aimed at medium-voltage and high-power applications. The CHBMLI is made by numerous H-bridge modules. For obtaining medium voltage level and lesser harmonics, the H-bridge modules are generally associated into series on AC side. The key benefits of a CHBMLI are its integrated construction in addition to being easy for replacement in the event of letdown. In order to feed these separate H-bridge power cell modules, large quantity of an isolated DC sources is needed in the CHBMLI. A discrete unit can produce three numerous levels of voltage like V_{dc}, 0 and -V_{dc} with the help of various groupings of switches. A seven-level CHBMLI can produce seven different levels of voltage like $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-2V_{dc}$ and $-3V_{dc}$ by means of three DC sources which is shown into Figure 1.

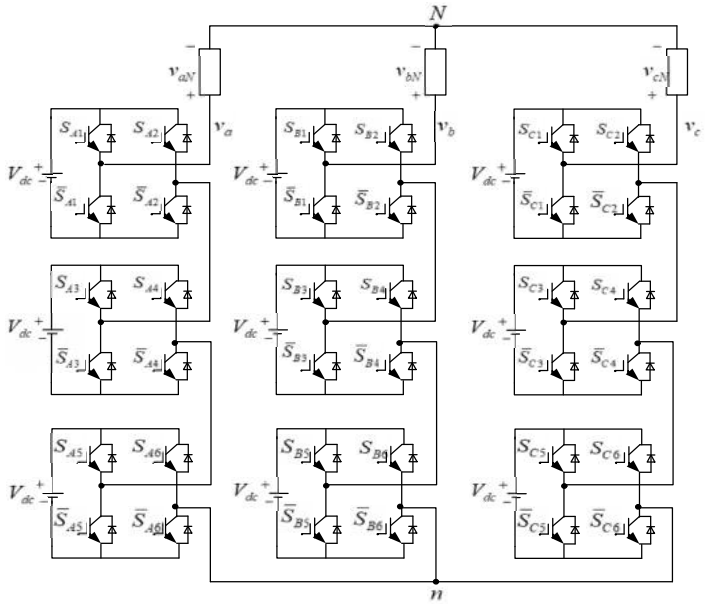

Figure 1. Seven-level cascaded multilevel inverter

3. PWM Techniques

The different modulation strategies are used for multilevel power conversion applications. The two widely used modulation strategies are SPWM and SVPWM strategy. In case of CHBMLI, mostly carrier-based PWM strategies are applied.

3.1 SPWM Method: There are two key types of carrier-based modulation strategies for the CHBMLI such as level-shifted and phase-shifted PWM. In case of the SPWM strategy, a sine modulating wave is compared with the vertically inclined carrier waves. In order to get seven-level voltage at the output we have to use six triangular carriers as shown in Figure 2. For all these carrier waves the magnitude and frequency are same. The magnitude of inverter output voltage is varied by using Amplitude Modulation Index (M_a). For multilevel inverters this M_a is given by,

$$M_a = \frac{V_m}{V_{cr}(m-1)} \tag{1}$$

Where, V_m represents modulating wave magnitude and V_{cr} represents individual carrier wave magnitude.

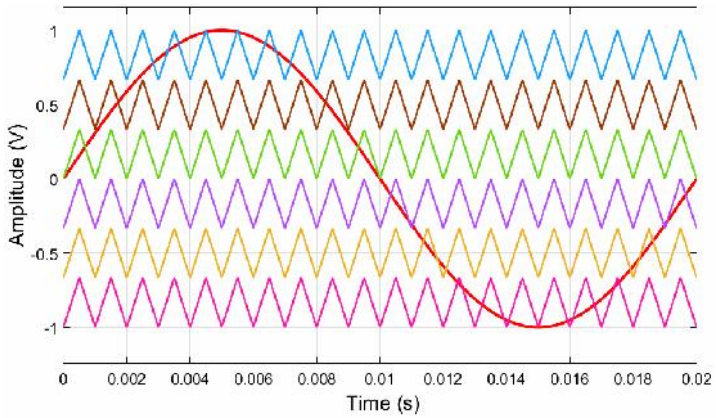

Figure 2. Sinusoidal reference wave and triangular carriers for a seven-level CHBMLI

3.2 Simplified SVPWM Method: The traditional SVPWM strategy wants large number of operating stages such as identification of sector number on the basis of reference voltage vector position, identification of triangle number, calculation of ON periods of active vectors after that a choice of redundant switching conditions, generation of switching sequence and finally to calculate the ON periods designed for every switching device. An innovative simplified SVPWM strategy is presented wherein the offset voltage has been included with reference phase voltages. The performance like traditional SVPWM method is obtain when we add this offset voltage with reference phase voltages, we obtain an extreme probable use of DC bus voltage.

$$V_{offset} = -\frac{(V_{\max} + V_{\min})}{2} \tag{2}$$

Where, V_{max} and V_{min} are highest and lowest amplitudes of the experimented reference phase voltages in the specific sample period. All dynamic switching vectors of a multilevel converter are gaining positioned in midpoint inside the specified sample interval with the addition of V_{offset} into the reference phase voltages. Figure 3 illustrated a simplified modulating signal and carrier waves. This modified space vector modulating signals are then compared with carrier waves so as to produce the gate pulses for IGBT switches.

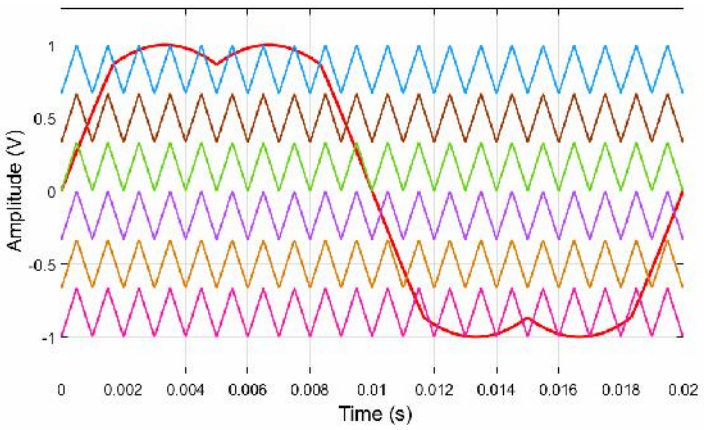

Figure 3. Space vector modulating wave and triangular carriers for a seven-level cascaded multilevel inverter

4. Simulation Results

A simulation has been performed in MATLAB software in order to show the usefulness of this new simplified SVPWM strategy. For simulation purpose, the seven-level CHBMLI having RL load is considered. The simulation is carried out for three different values of amplitude modulation index (M_a). For these three different values of M_a, line voltages of the seven-level CHBMLI are attained distinctly for the SPWM and simplified SVPWM strategy together with their harmonic spectrum. The parameters of simulation are stated inside Table 1.

Table 1. Parameters of simulation

Parameter	Value
DC bus voltage	600 V
Switching Frequency	1050 Hz
Resistive load per phase (R)	50 ohms
Inductive load per phase (L)	20 mH

4.1 Simulation results of the seven-level CHBMLI with SPWM strategy: Figure 4 illustrated the scheme of SPWM strategy aimed at a seven-level CHBMLI. Figure 5 shows the seven-level cascaded multilevel inverter line voltage in case of M_a=1 with a SPWM strategy and Figure 6 illustrated their corresponding harmonic spectrum. Figure 7 illustrated the seven-level cascaded multilevel inverter line voltage in case of M_a=0.8 with a SPWM strategy. Figure 8 illustrated corresponding harmonic spectrum.

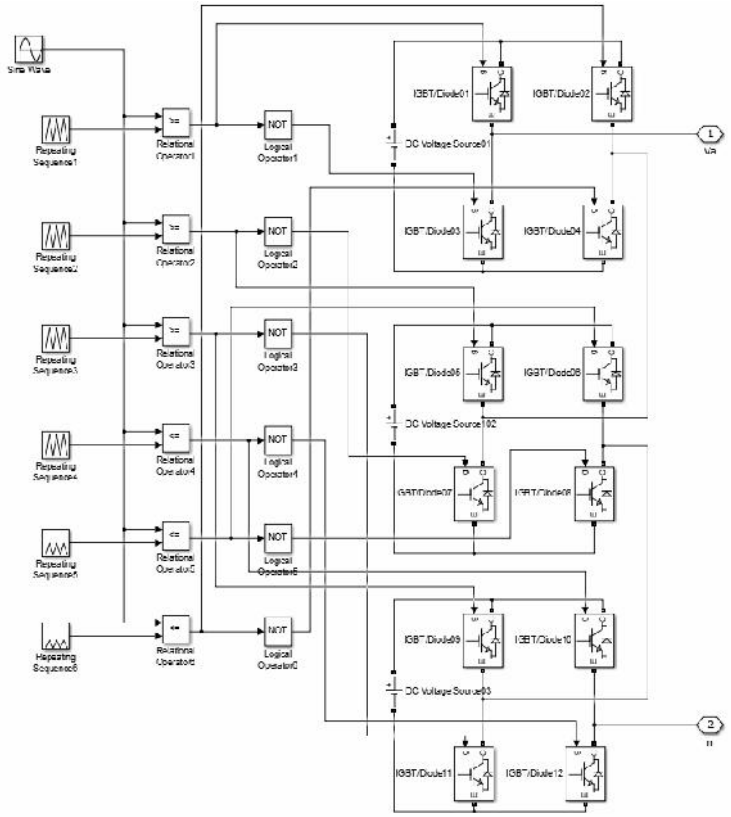

Figure 4. Scheme of the seven-level CHBMLI with SPWM strategy

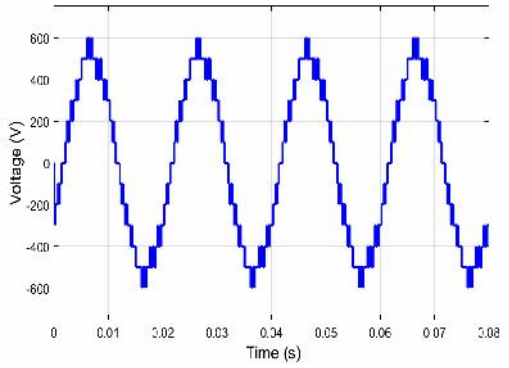

Figure 5. Seven-level cascaded multilevel inverter line voltage in case of M_a=1

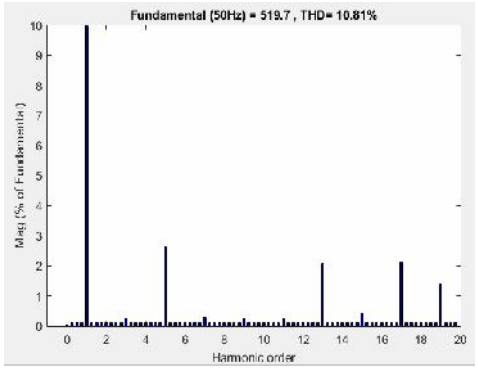

Figure 6. Seven-level cascaded multilevel inverter line voltage THD in case of M_a=1

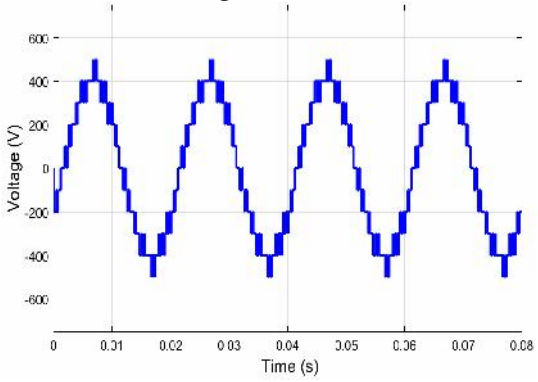

Figure 7. Seven-level cascaded multilevel inverter line voltage in case of M_a=0.8

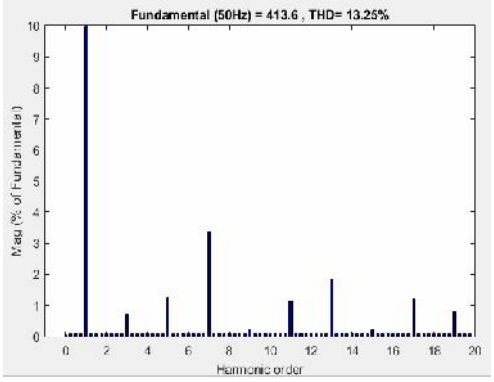

Figure 8. Seven-level cascaded multilevel inverter line voltage THD in case of M_a=0.8

Figure 9 illustrated the seven-level cascaded multilevel inverter line voltage in case of M_a=0.6 with a SPWM strategy. Figure 10 illustrated their corresponding harmonic profile.

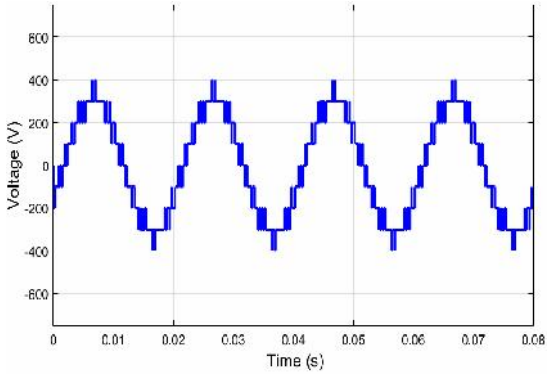

Figure 9. Seven-level CHBMLI line voltage for M_a=0.6

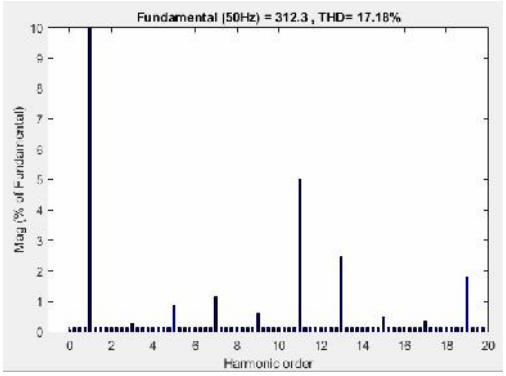

Figure 10. Seven-level CHBMLI line voltage THD for M_a=0.6

4.2 Simulation results of the seven-level CHBMLI with modified SVPWM strategy: The simulation block in order to generate modified SVPWM reference waves is demonstrated in Figure 11. Figure 12 shows a seven-level cascaded multilevel inverter line voltage in case of M_a=1 with a modified SVPWM strategy. Figure 13 illustrated corresponding harmonic profile.

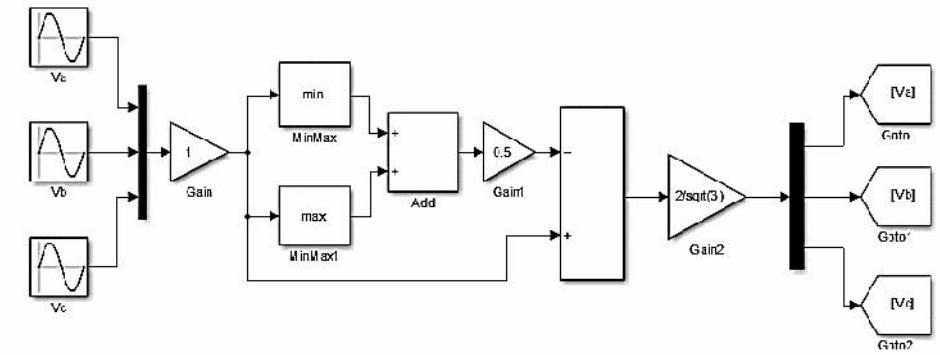

Figure 11. Simulation block in order to generate modified SVPWM reference waves

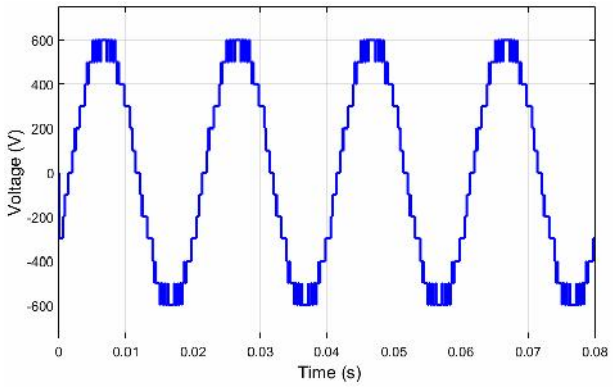

Figure 12. Seven-level CHBMLI output line voltage in case of M_a=1

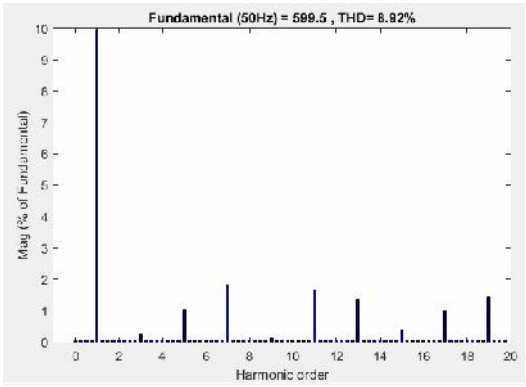

Figure 13. Seven-level cascaded multilevel inverter line voltage THD in case of M_a=1

Figure 14 illustrated a seven-level cascaded inverter line voltage in case of M_a=0.8 with a simplified SVPWM strategy. Figure 15 illustrated their corresponding harmonic profile.

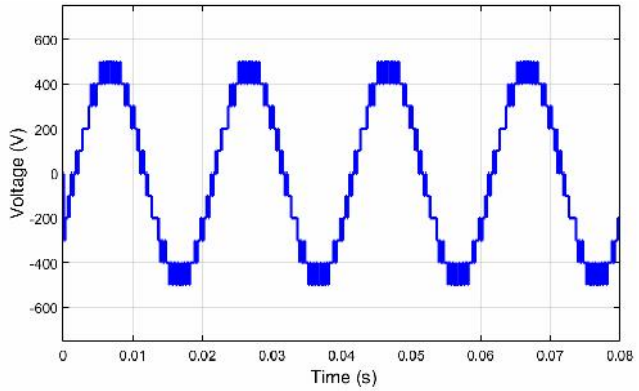

Figure 14. Seven-level CHBMLI output line voltage in case of M_a=0.8

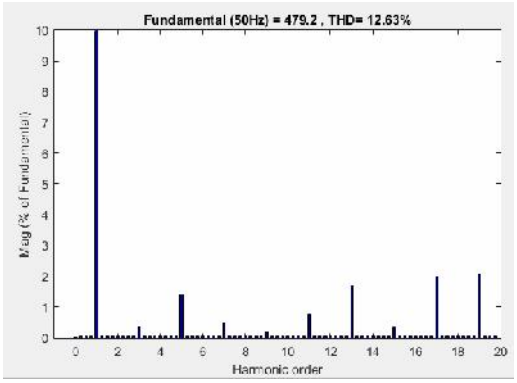

Figure 15. Seven-level CHBMLI line voltage THD for M_a=0.8

Figure 16 displays a seven-level cascaded inverter line voltage in case of M_a=0.6 with a simplified SVPWM strategy. Figure 17 illustrated corresponding harmonic profile.

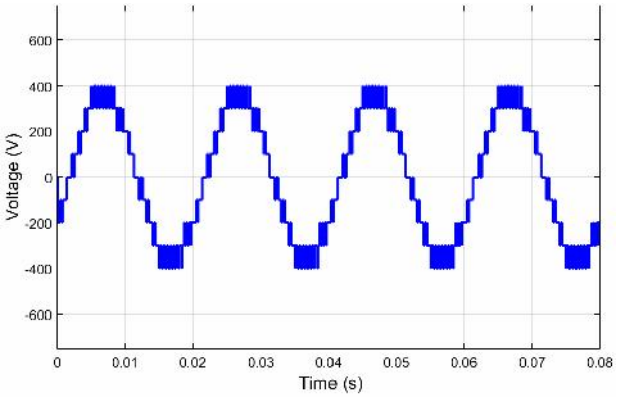

Figure 16. Seven-level CHBMLI output line voltage in case of M_a=0.6

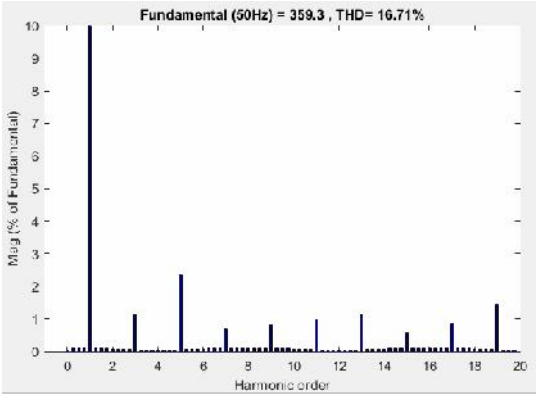

Figure 17. Seven-level CHBMLI line voltage THD for M_a=0.6

Table 2. Comparative study of modified SVPWM strategy with SPWM strategy

Modulation Index (M_a)	SPWM		Simplified SVPWM	
	THD in Line Voltage (%)	Fundamental Voltage Component	THD in Line Voltage (%)	Fundamental Voltage Component
1	10.81	519.7	8.92	599.5
0.8	13.25	413.6	12.63	479.2
0.6	17.18	312.3	16.71	359.3

When a seven-level cascaded inverter is operated by the modified SVPWM strategy, we obtain higher fundamental voltage component into the line voltages as shown in the simulation results as compared with a SPWM strategy as a result of enhanced DC bus voltage use. As well as, the harmonics are also reduced with a modified SVPWM strategy as compared to the SPWM strategy as stated inside Table 2.

5. Conclusion

In this paper, an innovative modified SVPWM strategy is applied to the seven-level CHBMLI. The new modified SVPWM strategy has disabled the downsides of classical SVPWM strategy as it does not need complicated and tedious calculations to

identify sector, to identify triangle and any look up tables. The comparative study is made among the novel modified SVPWM strategy and SPWM strategy. The simplified SVPWM strategy offers more fundamental voltage component in output line voltage as a result of improved DC bus voltage use than the SPWM strategy. As well as, the harmonics are reduced in seven-level cascaded inverter output line voltage with the modified SVPWM strategy than SPWM strategy. The novel modified SVPWM strategy offers complete benefits as like traditional SVPWM strategy.

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Biographical notes

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