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A 15-level asymmetric H-bridge multilevel inverter using d-SPACE with PDPWM technique

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Abstract

Multilevel Inverter is an energy conversion device that is generally used in medium voltage and high power applications. It offers lower total harmonic distortion, switching losses, voltage stress on switches than conventional inverter. This paper presented a 15 level asymmetric H-bridge multilevel inverter using a topology with less number of switches. In asymmetrical MLI, DC source magnitudes are unequal and it is designed as to maintain a ratio of 1:2:4. The modulation technique that has been used here to get proper switching is PDPWM. The input PWM signals have been generated using MATLAB Simulink and real time simulation and subsequent interface with hardware has been done using d-SPACE and MicroLab Box (DS-1202). A 2kHz multiple carrier signal is used to develop phase disposition pulse width modulation (PD-PWM).A study of this modulation technique used has been done and received results provides better efficiency , less low order harmonics and less switching loss.

Keywords: Multi-Level Inverter (MLI), Phase Disposition Pulse Width Modulation (PD-PWM), Fast Fourier Transform (FFT), Total Harmonic Distortion (THD).

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1. Introduction

The concept of MLI was introduced in 1975. The term 'multilevel' began with the three level converter. A multilevel converter is a power electronic system that synthesizes a desired output voltage from several levels of DC voltages as inputs (Prathiba *et al.*, 2010; Vijayalakshmi *et al*,. 2015; Thombre *et al*., 2014). With an increasing number of DC voltage sources, the converter output voltage waveform approaches a nearly sinusoidal waveform, while using a fundamental frequency switching scheme. In recent years, a great number of industrial applications have begun to request high power instruments. A source in medium voltage level is inconvenient to directly connect only one switching device. Consequently, the multilevel inverter topology has emerged as a different option for working with medium voltage and high power (Rajesh *et al.*, 2016). Multilevel inverters have received added awareness for their ability on high power and medium voltage function, and because of their ability to provide high power quality, lower order harmonics switching losses and improved electromagnetic interference (Chacko S *et al*. 2014). Figure 1 shows the classification of multilevel inverter topologies. Basically, MLIs are able to make different number of voltage levels at the output as a stepwise waveform by contribution of using multiple counts of active switches, passive power diodes and some DC voltage sources which can be either Photovoltaic (PV) panels or other renewable energy supplies or even from batteries (BhanuTej *et al*., 2018). The neutral-point-clamped converter (NPC) (Nabae *et al*., 1981), flying capacitor converter (FC) (Corzine *et al*., 2003), and Cascade H Bridge (CHB) are the most common multilevel topologies available. Multilevel inverters are one of the best option for medium and high power applications (Bendre *et al.*2006). Several H bridge are connected in series to get multilevel stepped waveform (Kouro *et al*., 2010; Rodriguez *et al*., 2002; Franquelo *et al*., 2008).

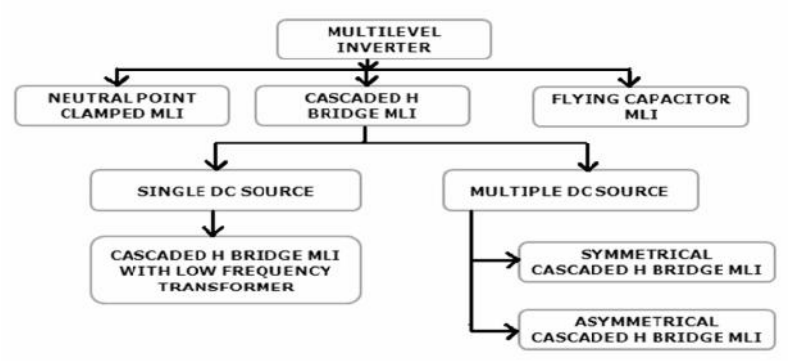

Figure 1. classification of multilevel inverters

Asymmetrical H-Bridge Multilevel Inverter:

In Kahwa *et al*. (2018), Gautam *et al*. (2018), a new hybrid topology of MLI with reduced number of switch is presented .In this paper, Level Shifted PWM topologies with reduced number of switches which uses the separate DC sources has been designed. In this topology the number of switches and number of levels are represented as follows

$$N\_Level = 2^{(n+1)} - 1$$

$$N\_MOSFET = n+4$$

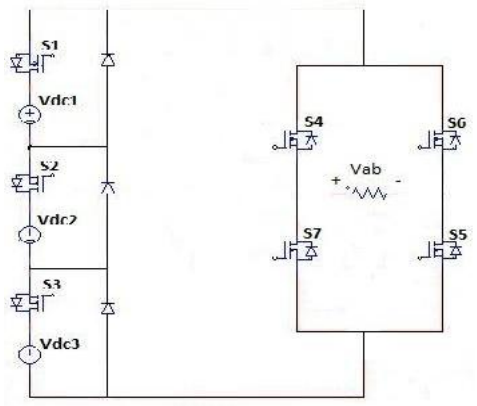

Figure 2. asymmetric h-bridge multilevel inverter

Where 'n' denotes the no. of dc sources. Here we can get up to 15 level output sine wave using only seven MOSFET switches and three DC voltage sources. Comparing with other topologies it is found that the Asymmetrical H-Bridge Multilevel Inverter topology uses the least no. of switches which effectively reduces the switching losses and circuit complexity. Figure 2 represents the Asymmetrical H-Bridge Inverter topology. In this inverter the DC source magnitude are unequal. The DC source magnitudes designed with binary form of voltage such as 3V, 6V and 12V respectively. Here the output voltage is 15 level and they are 21V, 18V, 15V, 12V, 9V, 6V, 3V, 0V,-3V,-6V,-9V,-12V,-15V,-18V and -21V respectively. In asymmetrical MLI, DC source magnitudes are unequal and it is designed as to maintain a ratio of 1:2:4. The major advantage of the asymmetric topology and its algorithms is associated to its ability to create a substantial number of output voltage levels by using low number of DC voltage sources and power switches.

2. Switching mode of operation for 15-level multilevel inverter

The 15 different levels of operation are shown in this section. Based on the gating signals, the three MOSFET switches in different times to create the different voltage levels. As we can see in Figure 2, there are three DC sources connected with three MOSFETS and every time the MOSFET connected with respective voltage sources gets the gate signal, it turns on. Then the DC sources provide the respective voltage level to the circuit. In Table 1, the switching pattern is shown with respect to each and every voltage level.

Table 1: switching order of mosfet based on gate signals

V_0	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**S7**
V_{DC}	1	1	1	1	1	0	0
$6V_{DC}/7$	0	1	1	1	1	0	0
$5V_{DC}/7$	1	0	1	1	1	0	0
$4V_{DC}/7$	0	0	1	1	1	0	0
$3V_{DC}/7$	1	1	0	1	1	0	0
$2V_{DC}/7$	0	1	0	1	1	0	0
$V_{DC}/7$	1	0	0	1	1	0	0
0	0	0	0	1	0	1	0
0	0	0	0	0	1	0	1
$-V_{DC}/7$	1	0	0	0	0	1	1
$-2V_{DC}/7$	0	1	0	0	0	1	1
$-3V_{DC}/7$	1	1	0	0	0	1	1
$-4V_{DC}/7$	0	0	1	0	0	1	1
$-5V_{DC}/7$	1	0	1	0	0	1	1
$-6V_{DC}/7$	0	1	1	0	0	1	1
$-V_{DC}$	1	1	1	0	0	1	1

2.1 Mode 1

Switch S1, S2, S3 & S4, S5 is ON, the voltage is maximum $+V_{dc}$ across the load which is shown in Figure 3.

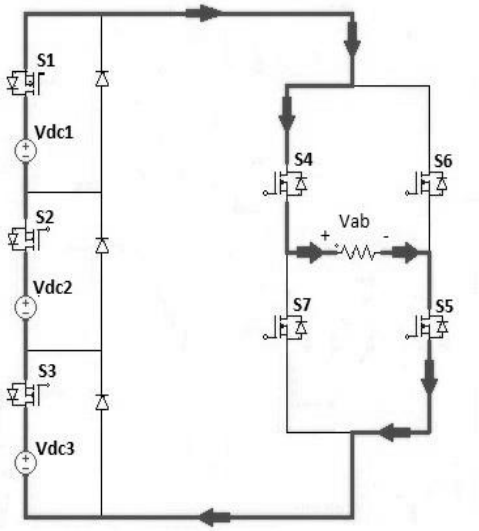

Figure 3. mode 1

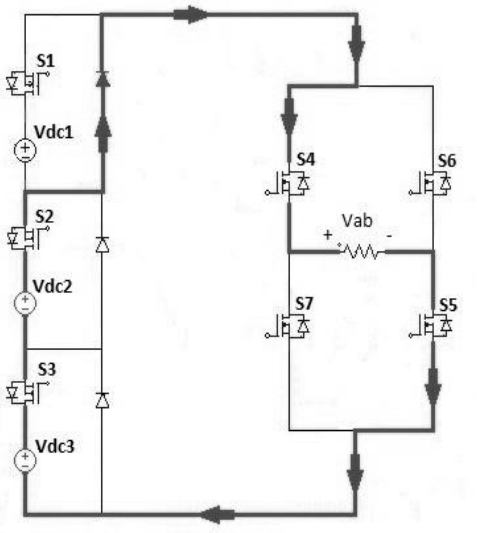

Figure 4. mode 2

2.2 Mode 2

Switch S2, S3 & S4, S5 is ON and the voltage is $+6V_{dc}/7$ across the load which shown in Figure 4.

2.3 Mode 3

Switch S1, S3 & S4, S5 is ON and the voltage $+5V_{dc}/7$ across the load which shown in Figure 5.

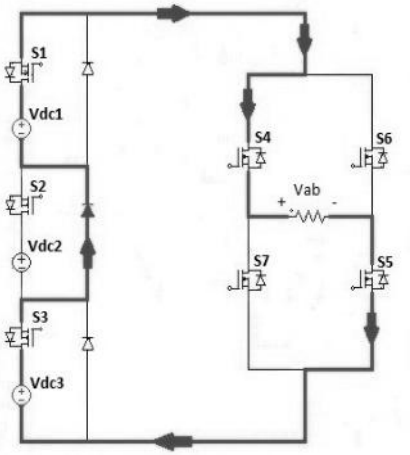

Figure 5. mode 3

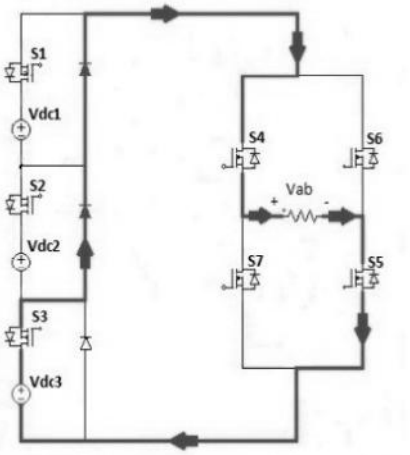

Figure 6. mode 4

2.4 Mode 4

Switch S3 & S4, S5 is ON and the voltage is $+4V_{dc}/7$ across the load which is shown in Figure 6.

2.5 Mode 5

Switch S1, S2 & S4, S5 is ON and the voltage is $+3V_{dc}/7$ across the load which is shown in Figure 7.

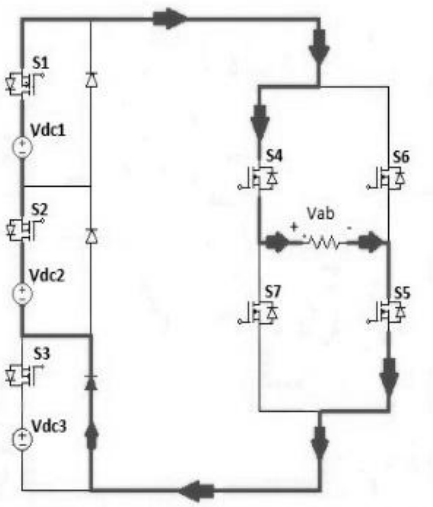

Figure 7. mode 5

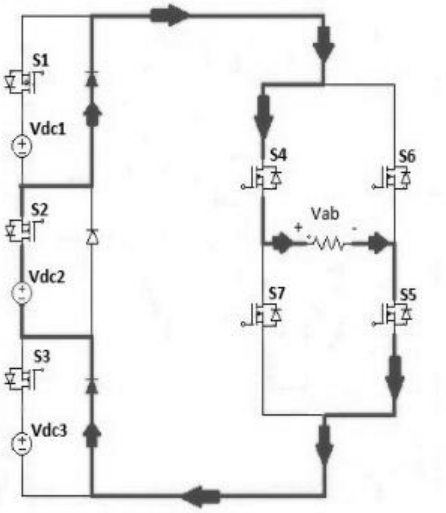

Figure 8. mode 6

2.6 Mode 6

Switch S2 & S4, S5 is ON and the voltage $+2V_{dc}/7$ across the load which is shown in Figure 8.

2.7 Mode 7

Switch S1 & S4, S5 is ON and the voltage $+V_{dc}/7$ across the load which is shown in Figure 9.

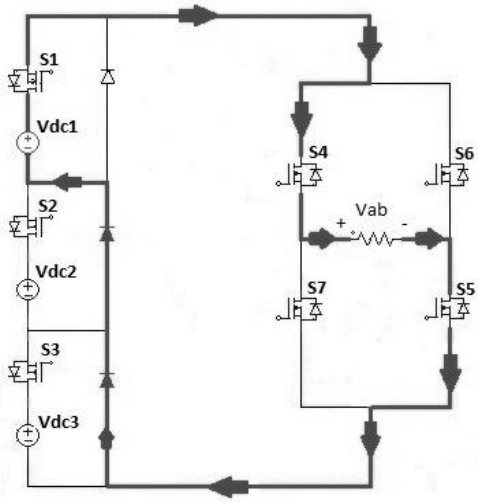

Figure 9. mode 7

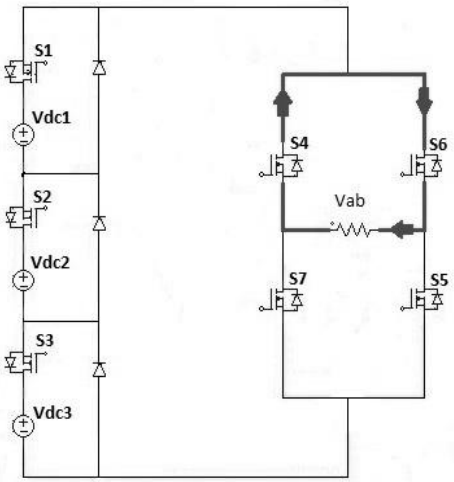

Figure 10(a). mode 8

2.8 Mode 8

The Zero Output voltage level is produced by turning ON MOSFET Switch S4 & S6 (Figure 10 (a)) or S7 & S5 (Figure 10 (b)] which is shown in the Figures 10(a) and 10 (b).

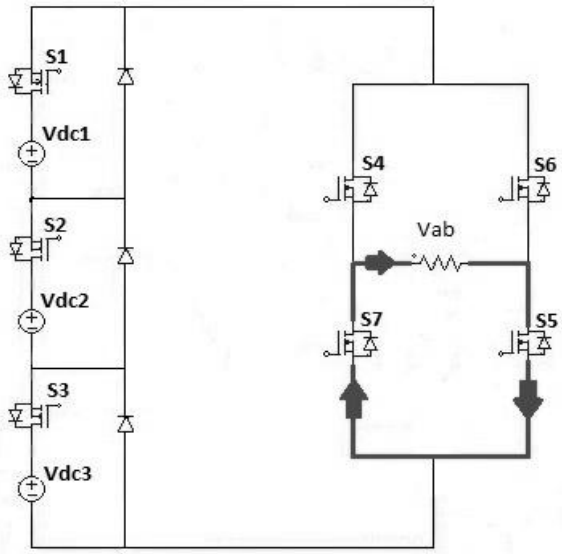

Figure 10(b). mode 8

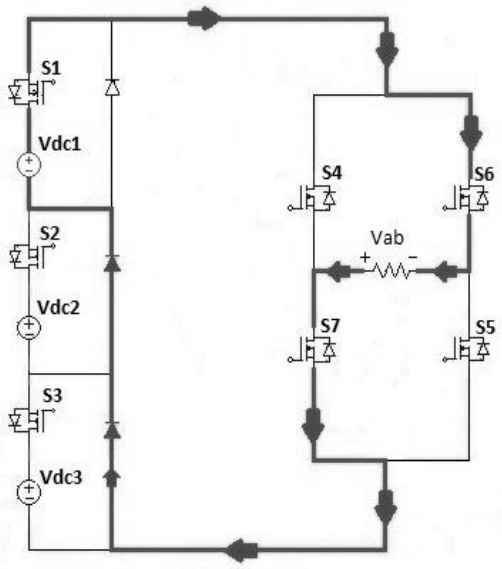

Figure 11. mode 9

2.9 Mode 9

Switch S1 & S6, S7 is ON and the voltage is $-V_{dc}/7$ across the load which is shown in Figure 11.

2.10 Mode 10

Switch S2 & S6, S7 is ON and the voltage $-2V_{dc}/7$ across the load which is shown in Figure 12.

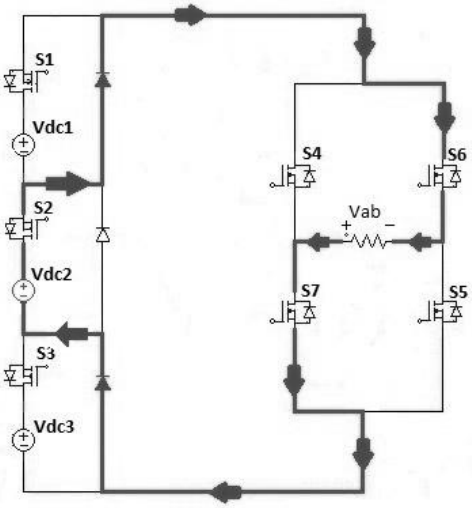

Figure 13. mode 11

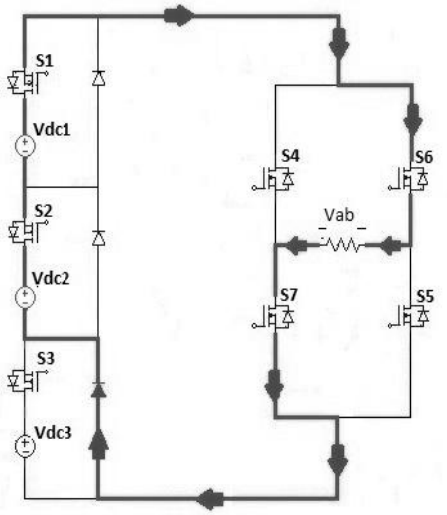

Figure 12. mode 10

2.11 Mode 11

Switch S1, S2 & S6, S7 is ON and the voltage $-3V_{dc}/7$ across the load which is shown in Figure 13.

2.12 Mode 12

Switch S3 & S6, S7 is ON and the voltage $-4V_{dc}/7$ across the load which is shown in Figure 14.

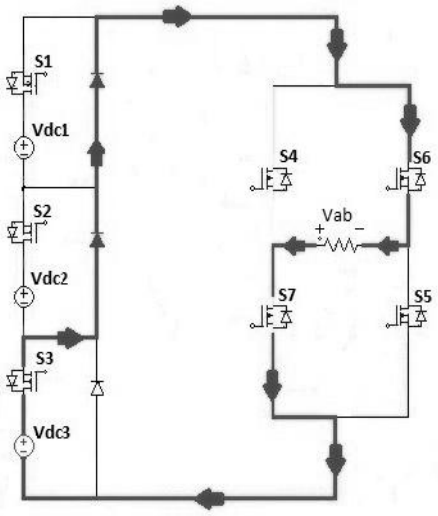

Figure 14. mode 12

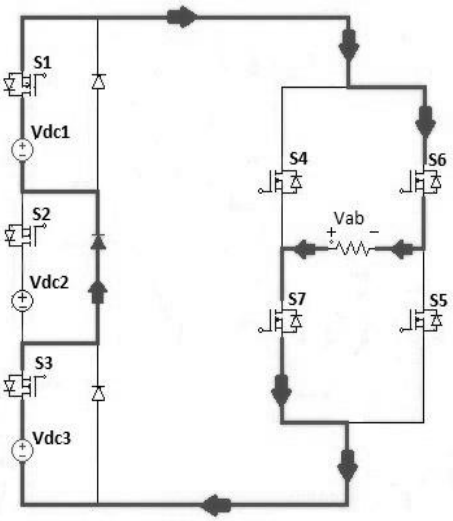

Figure 15. mode 13

2.13 Mode 13

Switch S1, S3 & S6, S7 is ON and the voltage $-5V_{dc}/7$ across the load which is shown in Figure 15.

2.14 Mode 14

Switch S2, S3 and S6, S7 is ON and the voltage $-6V_{dc}/7$ across the load which is shown in Figure 16.

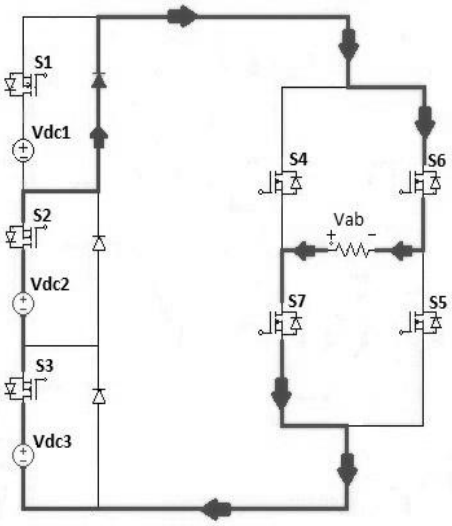

Figure 16. mode 14

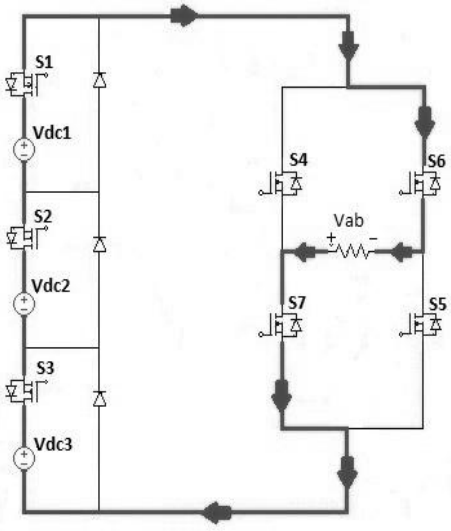

Figure 17. mode 15

2.15 Mode 15

Switch S1, S2, S3 & S6, S7 is ON and the voltage $-V_{dc}$ (negative maximum) across the load which is shown in Figure 17.

3. Modulation technique

The output voltage of the inverter can be adjusted by exercising a control within the inverter itself. The most efficient method of doing this is by Pulse Width Modulation (PWM) control used within the inverter [2]. In this method, a fixed DC input voltage is given to the inverter and a controlled AC output voltage is obtained by adjusting the ON-OFF periods of the inverter components. This is the most popular method of controlling the output voltage and this method is termed as PWM control. In this project, *Phase Disposition Pulse Width Modulation* has been used. This topology comes under Level Shifted PWM topology.

Phase disposition pulse width modulation:

This is a level shifted multiple carrier pulse width modulation technique. In Phase Disposition PWM or PDPWM, all carrier signals are in same phase as shown in Figure 18.

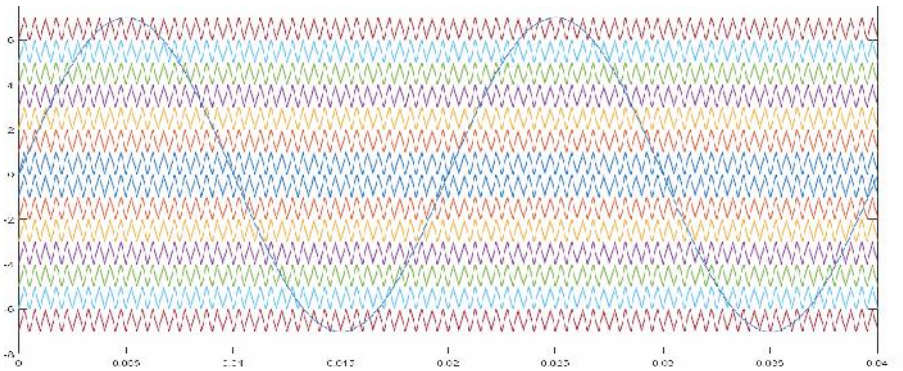

Figure 18. pd-pwm technique

The technique uses a Sinusoidal wave of frequency 50 Hz as the reference signal that is compared with triangular carrier waves of frequency 2 kHz. The resultant PWM output then acts as gate driver signal for the MOSFETS.

4. Simulations and results

The circuit diagram simulated in MATLAB is shown in Figure 19(a) & 19(b).

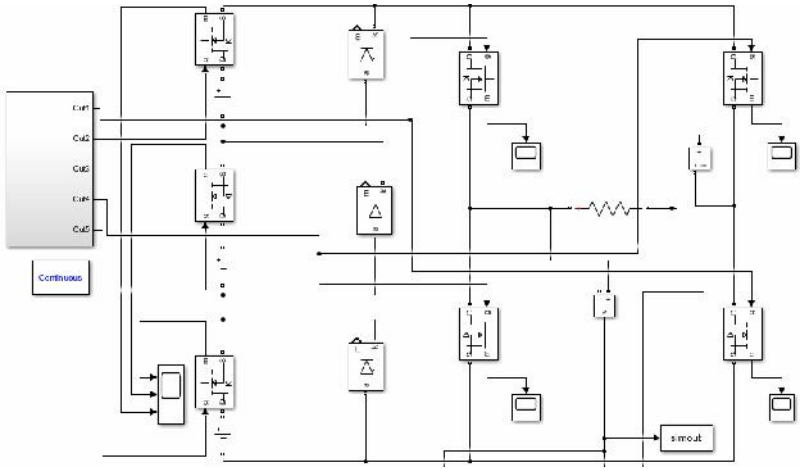

Figure 19(a). matlab circuit diagram

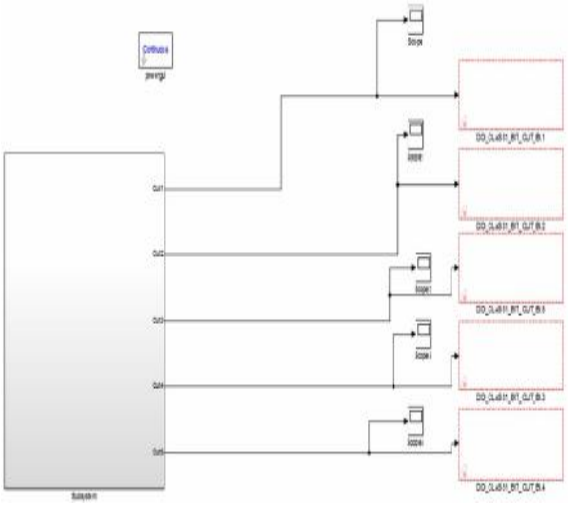

Figure 19(b). subsystem block linked to d-space

The PWM control signals are generated within a block subsystem and are fed to the gates of each MOSFET respectively. The signals generated using subsystem are shown in Figure 20 & 21.

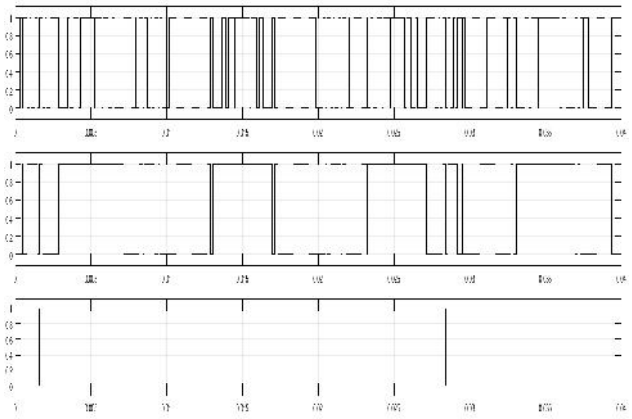

Figure 20. switching pulses for s1, s2 and s3 (pd-pwm)

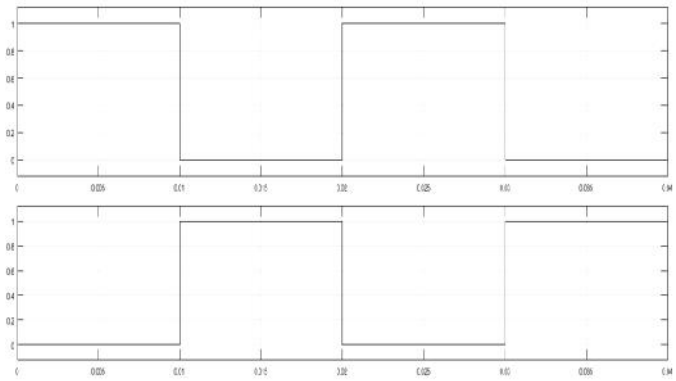

Figure 21. switching pulses for h-bridge

The MATLAB circuit is tested using different loads like resistive load of 470Ω and R-L load of 470Ω, 20 mH and the changes in the results are observed and analyzed. The following results will show how the output voltage and current waveforms are affected in the case of R loading and R-L loading.

We have also done the THD analysis for both Voltage and current waveforms and presented them in the following sections so as to see the effects of change in loading.

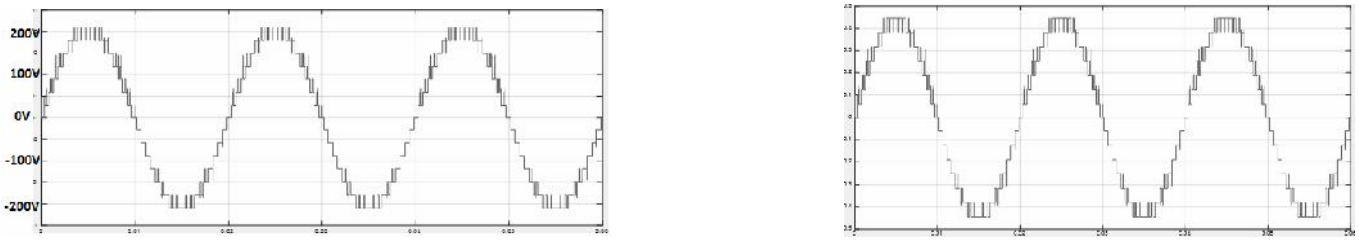

Figure 22. voltage waveform and current waveform with 470 ohms resistance

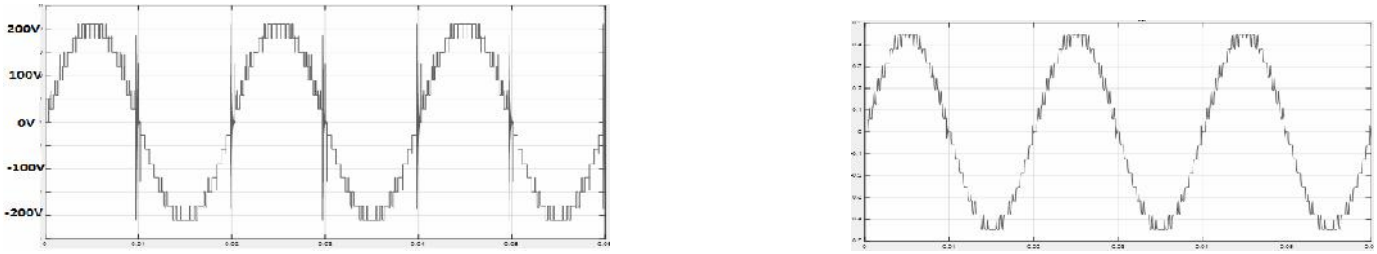

Figure 23. voltage waveform and current waveform for RL load

THD Analysis-

The total harmonic distortion is analyzed in this segment followed by the results we get from the MATLAB

The voltage and current THD is shown is shown in the Figure 24 & 25 for resistive load (470 ohms) –

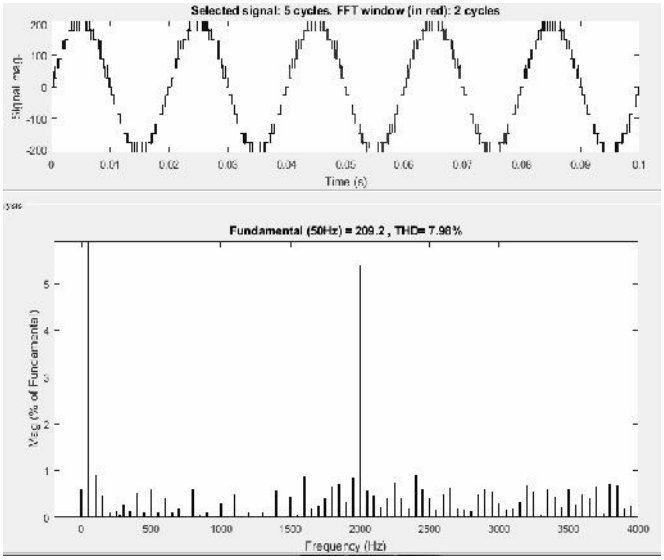

Figure 24. voltage thd for resistive load (470 ohms)

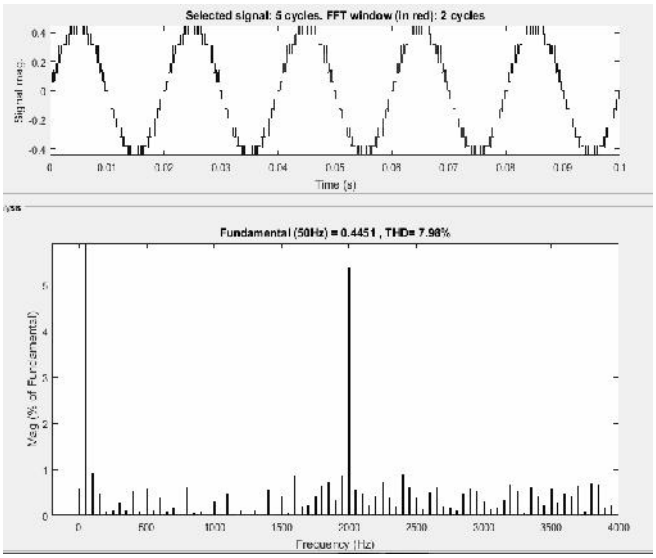

Figure 25. current thd for resistive load (470 ohms)

The voltage and current THD is shown is shown in the Figures 26 & 27 for RL load (470 ohms, 20mH) –

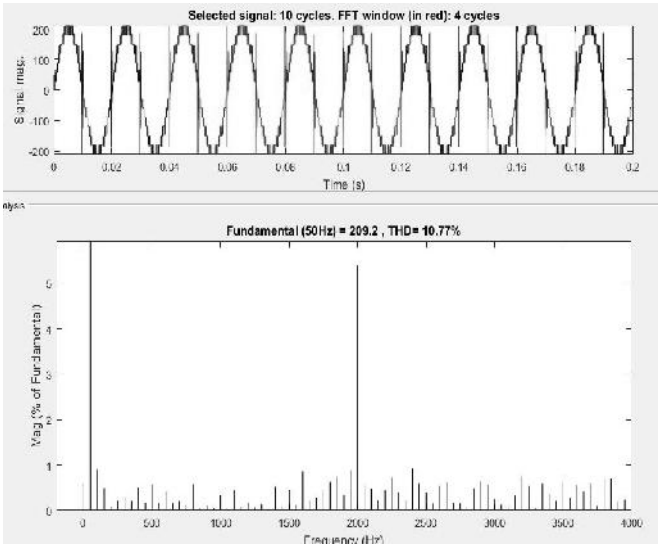

Figure 26. voltage thd for RL load (470 ohms, 20mh)

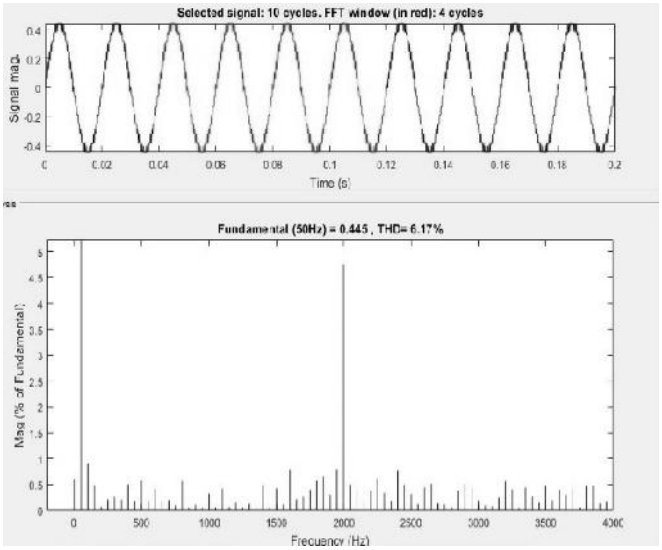

Figure 27. current thd for RL load (470 ohms, 20mh)

5. Hardware results

In order to make the real time interface, the above subsystem is used in dSPACE software. MicroLab Box, an FPGA processor platform with capability of processing up to 2GHz frequency, has been used to link software to hardware. The signals from MicroLab box as obtained in a DSO is shown in Figure 28.

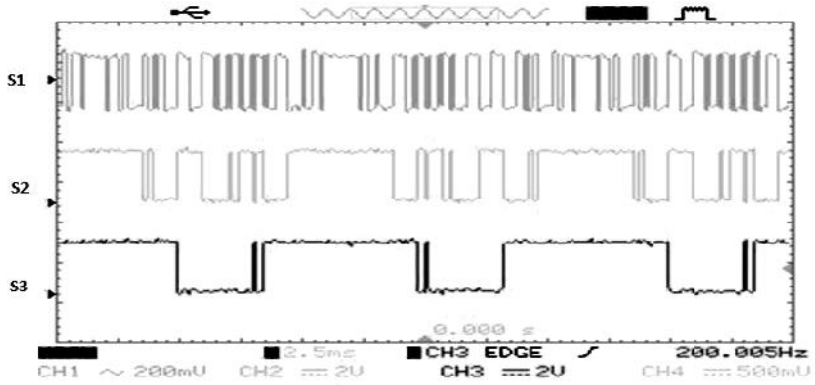

Figure 28. DSO output from microlab box

We have used three dc voltage sources of magnitude 3V, 6V, 12V and connected a 1 kΩ load for test purpose and obtained the following results.

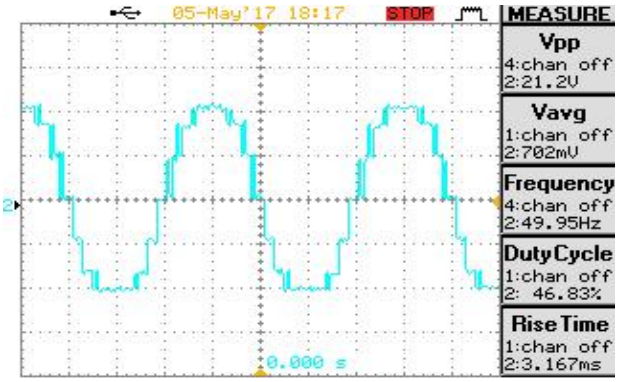

Figure 29. output voltage waveform of hardware circuit

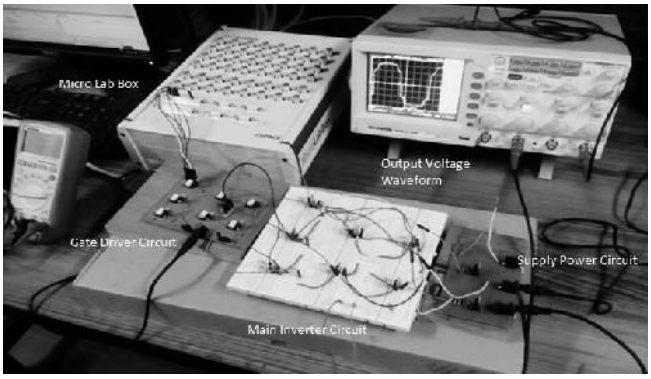

Figure 30. total hardware circuit

6. Conclusion

The proposed multilevel inverter topology with reduced number of switches can be implemented for industrial drive applications with renewable energy resources. The basic operation of the proposed multilevel inverter topology and the mechanism to obtain the required voltage level on each stage has been discussed elaborately. For the same fifteen levels, the conventional inverters employ with more number of switches which increases switching losses, cost and circuit complexity. But, in the proposed inverter topology only seven switches are used which overcomes these disadvantages as mentioned in the table 2 . Moreover it effectively diminishes lower order harmonics. Therefore effective reduction of total harmonic distortion is achieved without using any filter circuit.

Table 2: Comparison of different 15 level asymmetric inverter topologies.

Components	Proposed Topology	CHB	NPC	FC
Main Power Switch	7	12	24	28
DC source	3	3	1	7
Diodes	3	0	60	0
Capacitor	0	0	12	0

The single phase level shifted PD-PWM switching technique is simulated in MATLAB/SIMULINK for various loads like R and RL. The real time switching pulses are generated by syncing the dSPACE software and MicroLab box DS1202 with the

SIMULINK model. The main advantage of using dSPACE software and MicroLab box DS1202 is that it reduces the complexity of using a microcontroller with suitable programming for generating the PWM signals.

Acknowledgement

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