MultiCraft

International Journal of Engineering, Science and Technology
Vol. 4, No. 1, 2012, pp. 55-64

INTERNATIONAL JOURNAL OF ENGINEERING, SCIENCE AND TECHNOLOGY

www.ijest-ng.com
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Power quality improvement in switched mode power supplies using two stage DC-DC converter

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Abstract

This paper deals with an improved power quality multiple output switched mode power supply (SMPS) using two stage DC-DC converter. A non-isolated buck-boost DC-DC converter is used as the first stage whereas single ended primary inductance converter (SEPIC) is used in the second stage. The first stage of buck-boost converter is designed in discontinuous conduction mode (DCM) for inherent power factor (PF) correction. Design and simulations of the two stage DC-DC converter with load variations on the SMPS are performed in MATLAB software to demonstrate the effectiveness of the multiple output DC-DC converter to have a stiff voltage regulation and negligible ripple.

Keywords: DC-DC converter; Two stage; PFC; THD; Buck-boost converter; SEPIC; SMPS; Power quality.

DOI: http://dx.doi.org/10.4314/ijest.v4i1.7S

1. Introduction

Multiple output DC-DC converters are desirable for a variety of applications to reduce the number of power supplies, complexity, space and cost than a large number of single output converters. Now a days, a DC-DC converter consisting of two stages is becoming popular as the use of first stage eliminates the second harmonic voltage effect that is reflected at the output because of single phase AC mains input (Zhu *et al*, 2005; Abe *et al*, 2003). The first stage converter can be a non-isolated DC-DC converter and the second stage should be an isolated DC-DC converter having multiple outputs. To reduce the complexity, cost and space, only a single output (the most sensitive one) is sensed and regulated by feedback control. Generally, in the front end, a diode bridge is used to convert AC mains voltage to unregulated DC voltage which results in poor power factor (PF). To compensate for this, in the present work, a DC-DC converter (Pressmen, 1998; Rashid, 2004) is used with power factor correction (PFC) circuit to meet the IEEE and IEC standards (IEEE 519, 1992; IEC 61000-3-2, 2004).

A non-isolated buck-boost converter capable of stepping up/down the input DC voltage is added as the first stage for the coarse regulation of the output voltage. Non-inverting buck-boost converter in boundary conduction mode is reported in the literature (Lin *et al*, 2010; Boora *et al*, 2008). In the second stage, a single ended primary inductance converter (SEPIC) is used with multiple outputs. The SEPIC is the preferred choice among the design engineers due to its low component count, simplicity, capability to operate in buck and boost modes of operation and to yield regulated output DC voltage with a cost-effective structure. The use of only one switch and relatively simple control required are strong reasons for the choice of the SEPIC as a second stage. The analysis of an isolated SEPIC using an inductor voltage detection technique is reported in (Tanitteerapan, 2004) where the voltage conversion ratio of the SEPIC is used for the operation of the control circuit. It is a very difficult task to control the voltages of a multiple output converter with different load ratings. The control of the multiple outputs in a DC-DC converter is discussed in various research papers (Singh, 2006; Jung *et al*, 2008). Most of these papers describe the simulations done in MATLAB software which is a widely accepted simulation tool (MathWorks, 2009).

In view of these issues, this investigation deals with the design and control of an improved power quality switched mode power supply (SMPS) using a two stage DC-DC converter to obtain completely regulated and isolated outputs. In the proposed two-stage

conversion process, a single phase non-isolated buck-boost converter is followed by the multiple output SEPIC that functions as the second stage. The circuit configuration, operation, analysis, and design of the proposed converter are presented for the SMPS. Finally, simulation results are presented to demonstrate the performance of the two stage DC-DC converter based SMPS during load and supply voltage variations.

2. Circuit Configuration and Analysis

Fig. 1 shows the circuit configuration of a SMPS using two stage DC-DC converter with second stage having multiple outputs. The AC supply is fed to a DBR (Diode Bridge Rectifier) which gives an uncontrolled DC voltage V_d to the DC-DC converter. First stage is a non-isolated buck-boost converter. It consists of a switch Sw1 for on/off control, an inductor L to store and release energy, a high frequency diode D_b and a filter capacitor C_o. When switch S_{w1} is ON, the inductor L stores energy and the capacitor C_o discharges across the load. When S_{w1} turns OFF, the inductor stored energy charges the capacitor and supplies the load through the diode D_b. As the inductance polarity is reversed when it transfers energy and hence the output voltage has a reverse polarity compared to the input side. The output voltage of the non-isolated buck-boost converter is sensed and compared with reference voltage V_{ref1} to generate the voltage error signal V_{e1}. This voltage error is given to a PI (Proportional - Integral) controller to nullify the error. A PWM signal is generated by comparing the output of the PI controller with a constant frequency ramp waveform which is given to the switch S_{w1} to control its duty ratio and hence regulated output voltage is obtained along with automatic current shaping.

The output of the first stage is given to the isolated SEPIC DC-DC converter. The SEPIC consists of an inductor L_1, a capacitor C_1, a switch S_{w2}, a magnetizing inductor L_m with primary winding N_p and five secondary windings N_{s1}, N_{s2}, N_{s3}, N_{s4},N_{s5} for the high frequency transformer (HFT), high frequency diodes D_1, D_2, D_3, D_4, D_5 and output filter capacitors C_{o1}, C_{o2}, C_{o3}, C_{o4}, C_{o5} respectively. A SEPIC stores the energy in an inductor, and transfers that energy to the output storage capacitor. This energy is released through the secondary windings when the switch S_{w2} is turned off. All the outputs are isolated from each other. One of the output voltage which is the most sensitive to the disturbances is sensed and compared with the reference voltage. The rest of the outputs are regulated by the duty cycle variation of the SEPIC which is determined by the control loop of the sensed output. The proper winding arrangements of the HFT lead to the control of all the output voltages. The voltage error V_{e2} (obtained from the feedback amplifier that amplifies the difference between the output voltage V_{o1} and the reference voltage V_{ref2}) is amplified in a PI controller, output of which is compared with a high frequency saw-tooth ramp, thus providing the pulses to the switch S_{w2}. By controlling the duty ratio, the power flow is controlled in a very efficient way. .

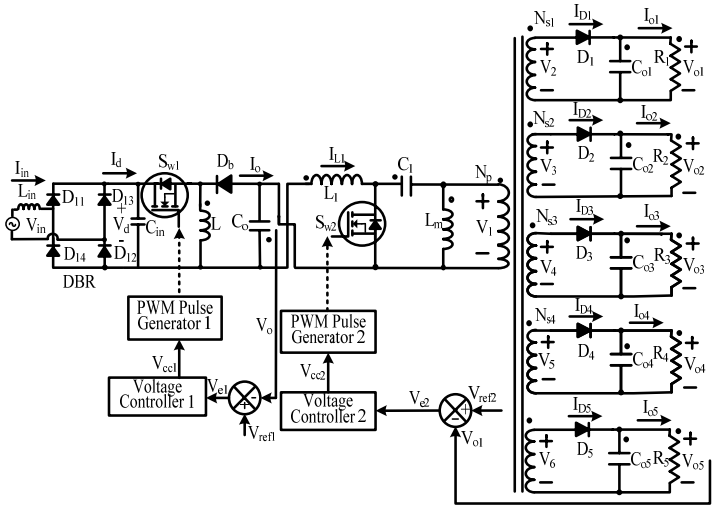

Figure1. Circuit configuration of improved power quality SMPS using two stage DC-DC converter

3. Design of Improved Power Quality Based SMPS Using Two Stage DC-DC Converter

In this section, the steady state analysis of the two stage DC-DC converter based SMPS is carried out to derive the required design equations for the converter. The two stage DC-DC converter can be viewed as a non-isolated DC-DC buck-boost converter cascaded with an isolated SEPIC. For the analysis, it is considered that the switches and diodes are ideal; the output filter capacitors are very large to keep the output voltage constant. The switching frequency is considered much higher than the line frequency so that average quantities in one switching cycle can be considered in place of instantaneous quantities. The HFT leakage inductance and stray capacitance are considered negligible.

3.1 Design of non-isolated buck-boost converter: The design of a non-isolated buck-boost converter is carried out in discontinuous

conduction mode (DCM) to avoid sensing of input current and voltage thus reducing the complexity. The voltage follower approach is used in the non-isolated buck- boost converter. When the switch S_{w1} is closed, the inductor current increases linearly; diode D_b remains in OFF condition. The change in the inductor current as,

$$(\Delta i_L)_{ON}=DT(V_d/L) \quad (1)$$

where V_d is the input voltage of the non-isolated buck-boost converter, $D=t_{on}/T$, T being the switching period of the converter, t_{on} being the ON time interval of S_{w1} and V_L is the voltage across the input inductor L.

When the switch is turned OFF and the diode D_b conducts, the inductor voltage is equal to the output voltage. So,

$$V_L=V_o=L\ (\Delta i_L)_{OFF}/(D_1T) \quad (2)$$

So, the change in the inductor current during OFF period may be written as,

$$(\Delta i_L)_{OFF}=V_oD_1T/L \quad (3)$$

where D_1 is less than (1-D)T for DCM i.e. OFF period of S_{w1} during which diode D_b is conducting.

The net change in the inductor current must be zero over one PWM period under steady state. Therefore, from eqns. (1) and (3),

$$(\Delta i_L)_{ON} + (\Delta i_L)_{OFF}=0 \quad (4)$$

Substituting eqn. (1) and eqn. (3) in eqn. (4),

$$DT(V_d/L)+ V_oD_1T/L =0 \quad (5)$$

Simplifying eqn. (5),

$$V_o/V_d= D/D_1 \quad (6)$$

The diode current is same as the output current during its conduction interval and hence,

$$I_o = I_m\ D_1T/(2T) \quad (7)$$

Where I_m is the maximum current that flows during the ON period. Therefore,

$$\Delta i_L=I_m= V_dDT/L \quad (8)$$

Substituting the value of I_m in eqn. (7), the D_1 is calculated as,

$$D_1= 2I_oL/(V_dDT) \quad (9)$$

The value of duty cycle D is considered as 0.645 for V_d=0.9* 220V=198V and V_o=360V. So from eqn. (6), D_1 is calculated as 0.34. So the inductor value from eqn. (1) is 1.04 mH for $I_o=P_o/V_o$=450W/360V=1.25A and the T=40µs. The second harmonic voltage is reflected on the output capacitor because of single phase AC mains feeding the buck-boost converter. To reduce the second harmonic voltage, the output filter is designed to maintain constant voltage at DC link and desired load current in all conditions. So the average value of the output current is,

$$I_o= V_dI_d/V_o \quad (10)$$

The charging current of the output capacitor is,

$$I_{co}(t)=(-V_d\ I_d\cos 2\omega t)/V_o = -I_o\cos 2\omega t \quad (11)$$

The output voltage V_o can be calculated as,

$$V_o= \frac{1}{C_o}\int I_c\,dt = -\frac{I_o}{2\omega C_o}\sin 2\omega t \quad (12)$$

The output voltage has ripples equal to the amplitude of the above relation. i.e.,

$$\Delta V_o=I_o/(2\omega C_o) \quad (13)$$

where I_o is the output current of the non-isolated buck-boost converter, ω is equal to 2*π*f, f is the fundamental frequency (50 Hz) and ΔV_o is the ripple of the output voltage.

The ripple in the output voltage can be kept low by selecting a large value of C_o which is given as,

$$C_o=I_o/(2\omega\Delta V_o) \quad (14)$$

From eqn. (14), substituting the output current I_o=450W/360V=1.25A, ω =314 rad/sec and ΔV_o=2% of the output voltage (7.2V), the value of output filter capacitor C_o is obtained as 270µF.

3.2 Design of SEPIC: The SEPIC is designed in continuous conduction mode to make the component values low. There is no need of sensing input current and input voltage as the output of first stage is DC voltage. In SEPIC, when the switch S_{w2} is ON, the inductor current changes as,

$$(\Delta i_{L1})_{ON} = V_oD_sT/L_1 \quad (15)$$

where V_o is the input voltage of the SEPIC which is the output from the first stage, D_s is the duty cycle of the SPEIC.

The change in inductor current, when switch S_{W2} turns OFF, is,

$$(\Delta i_{L1})_{OFF} =\{V_o-V_{C1}-V_{o1}(N_p/N_{s1})\}/L_1\}(1-D_s)T \quad (16)$$

where N_p and N_{s1} are the number of turns of the primary winding and secondary windings of the HFT, $n=(N_{s1}/N_p)$ is the turns ratio of HFT, V_{c1} is the voltage across the capacitor C_1 and V_{o1} is the output voltage of SEPIC.

Under steady state condition the change in the inductor current is zero over a period T as,

$$(\Delta i_{L1})_{ON} + (\Delta i_{L1})_{OFF}=0 \quad (17)$$

Substituting eqn. (15) and eqn. (16) in eqn. (17),

$V_oD_sT/L_1+ V_o-V_{C1}-V_{o1}(N_p/N_{s1})\}/L_1\}(1-D_s)T=0$ (18)

On solving eqn. (18), we obtain

$V_{o1}/V_o = nD_s/(1-D_s)$ (19)

From eqn. (19) it can be seen that the output voltage of the SEPIC can be varied by adjusting the duty ratio of the switch (D_s) and the HFT turns ratio (n). The duty cycle is considered as 0.45 for its optimum operation, so from eqn. (19) the turns ratio 'n' is calculated as 0.0407 for V_o=360V,V_{o1}=12V.

The input inductor value L_1 can be calculated for a given value of its ripple current. During the ON period the inductor current increases linearly.

$L_1=V_oD_s/(f_s\Delta i_{L1})$ (20)

The value of the inductor L_1 from eqn. (20) is computed to be 15mH for a ripple current of 10% (0.204A) and a switching frequency of f_s=50 kHz.

The value of capacitor C_1 for a given value of ripple voltage is, $C_1 = nV_{o1}D_s/(R_1f_s\Delta V_{C1})$ (21)

According to eqn. (21), the value of capacitor C_1 is computed as=400μF for V_{o1}=12V, D_s=0.45, R_1=12V/15A=0.8 Ω and f_s=50 kHz.

The output voltage ripple (ΔV_{o1}) is calculated during ON period, in which output capacitor (C_{o1}) is discharged through load. Thus the output voltage ripple is,

$\Delta V_{o1} = V_{o1}D_sT/(R_1C_{o1})$ (22)

The value of output capacitor (C_{o1}) can be calculated from eqn. (22) for a given ripple voltage (ΔV_{o1}) as,

$C_{o1} = V_{o1}D_s/(f_sR_1\Delta V_{o1})$ (23)

The output filter capacitor C_{o1} value is calculated as 560μF for V_{o1}=12V, D_s=0.45, R_1=12V/15A=0.8 Ω, f_s=50 kHz and ΔV_{o1}=2% (0.24V). The design equations used in the designing of the converter are based on the derivation of the output of the highest rating with the input. For rest of the outputs, the equations are derived using the HFT turns ratio. The other output voltages, components value are calculated by using the same design equations which are as follows: C_{o2}= 2.8mF, C_{o3}= 4.09mF, C_{o4}= 30μF, C_{o5}= 27μF for V_{o2}=5V, V_{o3}=3.3V, V_{o4}=-12V, V_{o5}=-5V, R_2= 5V/30A=0.16Ω, R_3=3.3V/30A=0.11Ω, R_4=-12V/0.8A=15Ω, R_5=-5V/0.3A=16.66Ω and ripple in the output voltages= 2% of the respective output voltages.

4. Control Algorithm

The control scheme for the two stage multiple output SMPS consists of voltage controllers and the PWM pulse generators. The control for non-isolated buck-boost converter and SEPIC are given in this section.

4.1 Control for Non-isolated Buck-Boost Converter: The non-isolated buck-boost converter is designed in DCM so that extra voltage/current sensors to sense input current and voltage can be avoided. A voltage follower control approach is chosen to regulate the output voltage of the converter. Initially the control loop computes the output voltage error and then the voltage error is given to a PI voltage controller and the output of this is further given to a PWM generator to obtain the ON/OFF control pulses.

4.1.1 Voltage Controller1: It consists of a PI controller which has two gains K_{p1} and K_{I1}. K_{p1} performs the proportional action while K_{I1} performs integral action. A PI controller gives control signal (V_{cc1}) to reduce the voltage error. At n^{th} instant of time, the voltage error $V_{e1}(n)$ is calculated as,

$V_{e1}(n)=V_{ref1}(n)-V_o(n)$ (24)

The controller output $V_{cc1}(n)$ at n^{th} instant is given as,

$V_{cc1}(n) = V_{cc1}(n-1)+K_{p1}\{V_{e1}(n)-V_{e1}(n-1)\}+K_{I1}V_{e1}(n)$ (25)

4.1.2 PWM Pulse generator1: In the PWM pulse generator, the fixed high frequency saw-tooth ramp is compared with the output of PI controller 1 (V_{cc1}) to get the PWM pattern for switch S_{w1}. When the saw tooth ramp is less than the output of the PI controller, the switch turns ON, else it is OFF.

4.2 Control for Isolated SEPIC: The control of SEPIC is carried out in continuous conduction mode (CCM) to reduce the stress of the components. Only one loop is required to regulate the output voltage as input voltage to the SEPIC is DC voltage. The control loop for SEPIC consists of only one PI voltage controller and PWM pulse generator**.**

4.2.1 Voltage Controller2: The PI voltage controller for SEPIC consists of two gains K_{p2} and K_{I2}. It gives the control signal (V_{cc2}) to reduce the voltage error i.e. the difference between actual voltage and the reference voltageV_{ref2}. At n^{th} instant of time, the voltage error $V_{e2}(n)$ is calculated as,

$V_{e2}(n)=V_{ref2}(n)-V_{o1}(n)$ (26)

The PI controller output $V_{cc2}(n)$ at n^{th} instant is given as,

$V_{cc2}(n)=V_{cc2}(n-1)+K_{p2}\{V_{e2}(n)-V_{e2}(n-1)\}+K_{I2}V_{e2}(n)$ (27)

4.2.2 PWM Pulse Generator2: The saw-tooth ramp is compared with the output of voltage PI controller 2, V_{cc2} to generate the PWM signal which is given to the switch S_{w2} of the SEPIC.

5. Modeling and Simulation

The model of the two stage DC-DC converter based SMPS is developed and its performance is simulated in MATLAB environment along with Simulink and Sim Power System toolboxes to validate the proposed design. This section describes the modeling and simulation of the proposed converter. Fig. 2 shows the simulation diagram of two stage DC-DC converter. Single phase AC supply is given to diode bridge rectifier and the output of the diode bridge rectifier is connected to a non-isolated buck-boost converter through a diode converter which is further fed to the second stage i.e. SEPIC. The secondary side of the HFT of SEPIC is having five outputs. One of the output which is more vulnerable to disturbance is sensed and compared with the reference voltage. The voltage error signal is given to a PI controller. The PWM generator generates the PWM signal which is given to the switch S_{w2}. The performance of the converter is studied for variations in the load. The design parameters used for the simulation of two stage DC-DC converter is summarized in the Appendix.

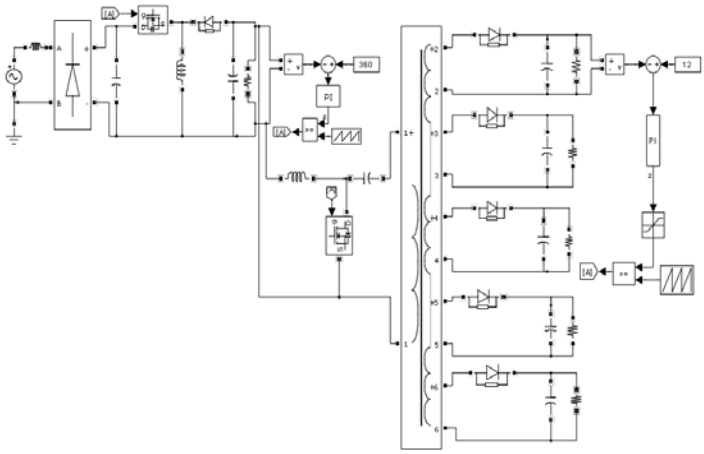

Figure 2. Simulation model of improved power quality SMPS

5. Results and Discussion

In this section, simulation results of an improved power quality SMPS using a two stage DC-DC converter are presented and discussed in detail. To study the performance of the SMPS and to check if various power quality indices are within specified limits, the proposed converter has been modeled, designed and simulated for the specifications given in Table I.

Simulation results of the two stage DC-DC converter based SMPS is presented to validate the design and control of the proposed configuration and to examine the various performance indices within IEEE standard 519 limit.

The simulated waveforms of the SMPS are shown in Figs. 3-10. Fig. 3 shows the supply voltage V_{in}, input current I_{in}, output voltages V_o, V_{o1}, V_{o2}, V_{o3}, $V_{o4,}$ V_{o5} and output currents $I_{o,}$ I_{o1}, I_{o2}, I_{o3}, I_{o4}, I_{o5} for a two stage DC-DC converter for a 433.5 W SMPS at full load (100% of load). From Fig. 3, it is clearly seen that the power factor is closed to unity as the input current follows the input voltage. Fig. 4 shows the harmonic spectrum of input mains AC current of the improved power quality SMPS using a two stage DC-DC converter at full load. The total harmonic distortion (THD) at full load is around 2.37% which is well within IEEE-519 standard limit. The input current and the input voltage are in phase and the power factor is very close to unity. The input voltage of the SMPS is varied from 220V to 270V and from 220V to 170V to demonstrate the performance of the SMPS under supply voltage variations. Fig. 5 shows V_{in}, I_{in}, V_o, V_{o1}; V_{o2}; V_{o3}; V_{o4}; V_{o5}, I_o, I_{o1}; I_{o2}; I_{o3}; I_{o4}; I_{o5} and Fig. 6 shows the harmonic spectrum of input mains AC current at 270V at full load condition. From Fig. 5, it is evident that the input current and input voltage are in phase and the THD of input AC mains current is 2.8%. The power factor is 0.9992 which is very close to unity. Similarly, Figs. 7 and 8 show the performance of improved power quality SMPS and harmonic spectrum of the input AC mains current respectively at 170V under full load. At supply voltage of 170V, the current THD is slightly high and the power factor is about 0.9977. Table II shows the various power quality indices of the improved power quality SMPS at different source voltages. To demonstrate the capability of the converter at varying loads, the load on the SMPS is varied in +12V output. Fig. 9 shows the performance of SMPS under the load variation on 12V output. The load is varied from 100% to 20% and then back to 100% to reveal the dynamic performance of the converter. The power factor is found to be 0.998 at 20% load and 0.9994 at 100% load. Fig.10. shows the harmonic spectrum of the input AC mains current of SMPS at 20% load on +12V output. Table III shows the

various power quality indices of the improved power quality SMPS at varying load conditions. It can be observed that the proposed two stage DC-DC converter based SMPS is able to deliver regulated and isolated outputs with improved power quality at the input AC mains under load and supply voltage variations.

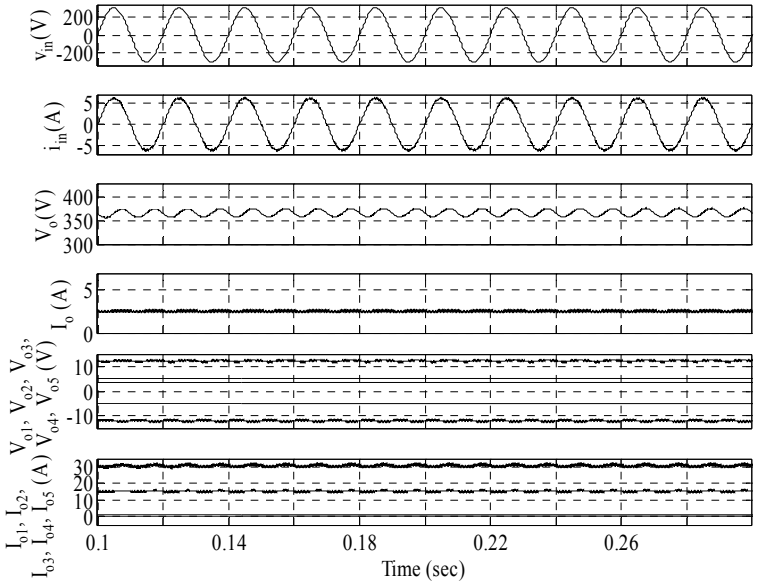

Figure 3. Input voltage, Input current, output voltages and output currents of improved power quality SMPS at 100% load

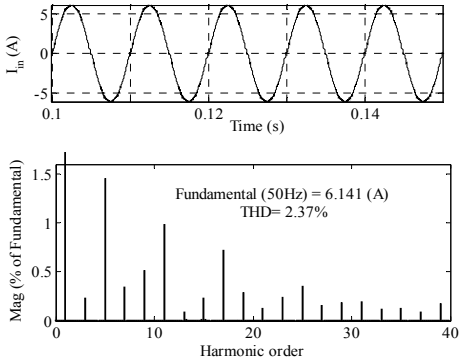

Figure 4. Input current waveform of SMPS and its harmonic spectrum at full load

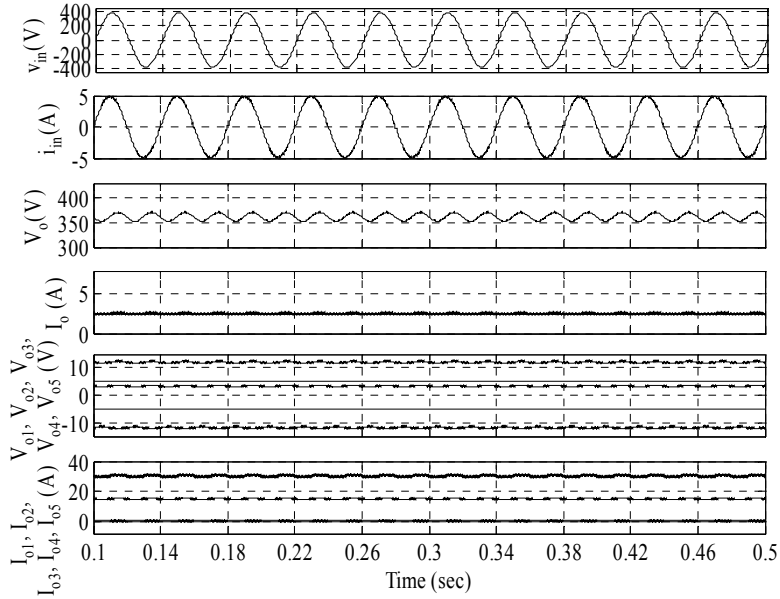

Figure 5. Input voltage, Input current, output voltages and output currents of improved power quality SMPS at 270V

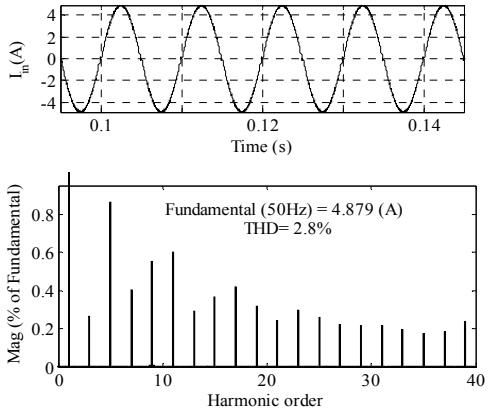

Figure 6. Input current waveform of SMPS and its harmonic spectrum at 270V

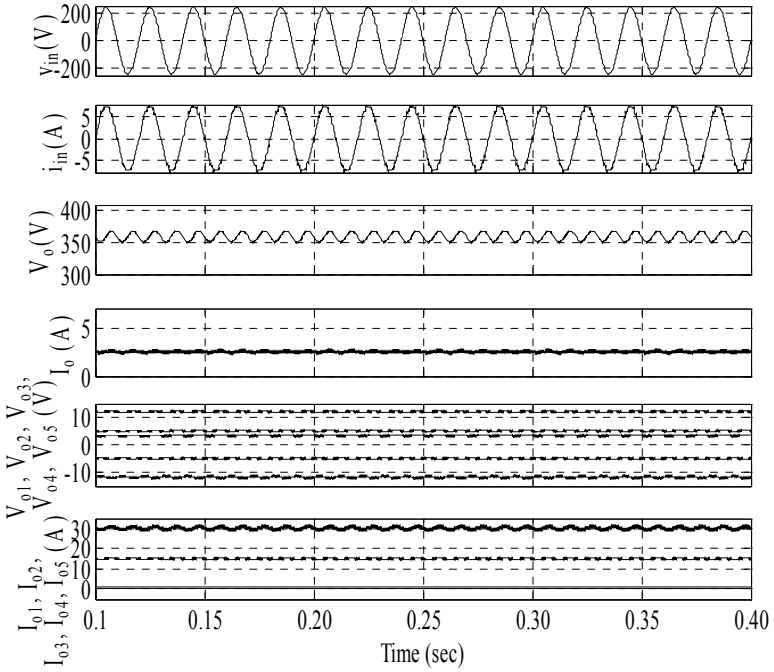

Figure 7. Input voltage, Input current, output voltages and output currents of improved power quality SMPS at 170V

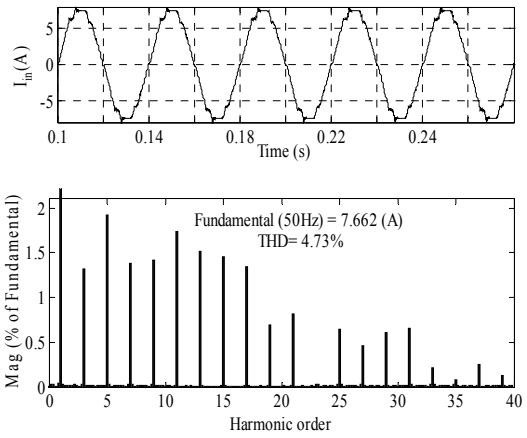

Figure 8. Input current waveform of SMPS and its harmonic spectrum at 240V

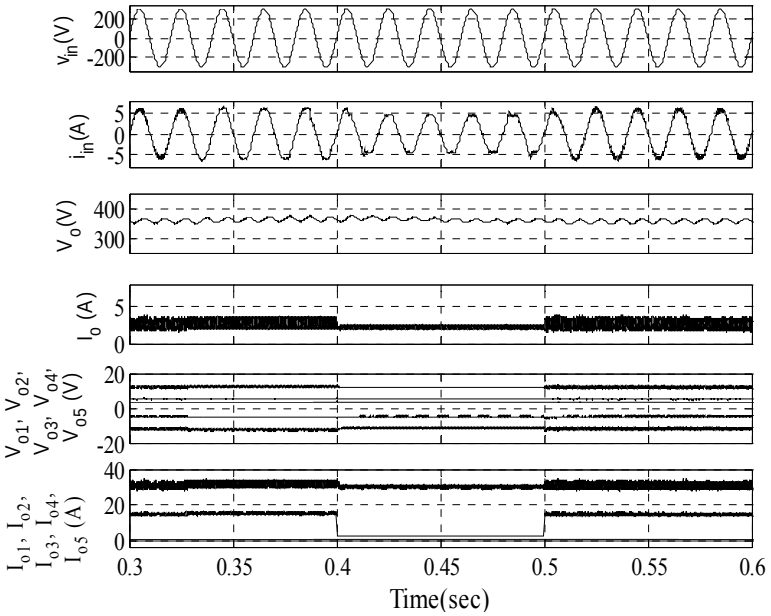

Figure 9. Input voltage, input current, output voltages and output current at 100% to 20% to 100% load variation in +12V output voltage

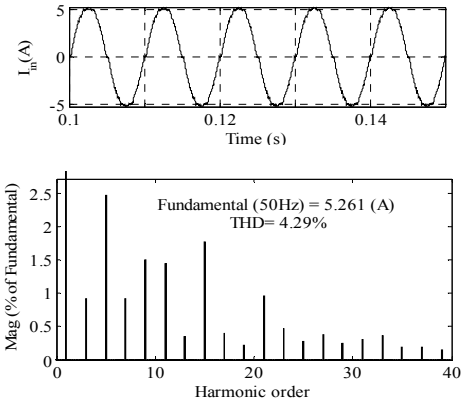

Figure 10. Input current of SMPS and its harmonic spectrum at 20% load

Table I
Improved power quality SMPS using two stage dc-dc converter specifications

Converter	Non-isolated buck-boost	SEPIC
Supply voltage	220V(rms)	360V
Output Voltage / Output Current	360/1.25A	12V/15A
		5V/30A
		3.3V/30A
		-5V/0.3A
		-12V/0.8A
Switching Frequency	25kHz	50kHz

6. Conclusions

An improved power quality SMPS using a two stage DC-DC converter has been designed and modeled and its performance has been simulated under varying supply voltage and load conditions. A single phase supply has been used for feeding the two stage DC-DC converter based SMPS. A voltage follower control approach has been used in the first stage converter to provide good output voltage regulation and power factor correction whereas the second stage is chosen to be a SEPIC. The proposed SMPS is found to yield unity power factor and very low THD at the utility interface while delivering stiffly regulated and isolated outputs. The performance of the SMPS is found to be excellent even under load variations and supply voltage variations adhering to IEEE 519 standard.

Table II
Power quality indices for the improved power quality SMPS using two stage dc-dc under varying source conditions

Input Voltage (V)	Input Current (A)	i_{THD} (%)	DF	DPF	PF
170	5.418	4.73	0.9977	1	0.9977
220	4.34	2.37	0.9994	1	0.9994
270	3.45	2.8	0.9992	1	0.9992

Table III
Power quality indices for the improved power quality SMPS using two stage dc-dc under varying loads conditions

Load (%)	i_{THD} (%)	DF	DPF	PF
20%	4.29	0.998	1	0.998
40%	4.01	0.9983	1	0.9983
60%	3.89	0.9984	1	0.9984
80%	3.10	0.9990	1	0.9990
100%	2.37	0.9994	1	0.9994

Appendix

Converter specifications: Input supply voltage: 220V (rms) 311V (peak), 50Hz;
DC output power: 433.5W (12V/15A, 5V/30A, 3.3V/30A, -5V/0.3A, -12V/0.8A)
Switching frequency: 25 kHz (for buck-boost converter), 50 kHz (for SEPIC)
K_{p1}=0.04, K_{I1}=3.5, K_{p2}= 0.89, K_{I2}=5.5.

Acknowledgement

Authors would like to acknowledge the Department of Science and Technology, Government of India for the research grant for the project entitled “Power Quality Improvement in Power Converter Systems” to carry out this research work.

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Received January 2012
Accepted February 2012
Final acceptance in revised form March 2012