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DUAL SLOPE INTEGRATION TECHNIQUE TO DESIGN A DIGITAL THERMOMETER

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ABSTRACT

A digital platinum resistance thermometer (PRT) is designed to measure temperature in the range of 0-200°C .

The analogue signal conditioning circuit of the system comprises the sensor (platinum wire), a deflection bridge and instrumentation amplifiers, while the digital circuit component was designed using a Dual-Slope Analogue-to Digital-Technique to process the d.c. signal with visual display. Facilities on ground however limited the range that was covered in this investigation to 0-90°C.

The prototype digital resistance thermometer was set up and test performance carried out to ensure linearity and accuracy of the system.

Keywords: Digital, dual-slope integration, thermometer, instru

1.0 INTRODUCTION

Physical quantities measured with electronic devices are transduced into electrical signals which are then processed and displayed. One of the many characteristics of such signals used to convey information is digital in form which represents a specified number that is related discontinuously, in integer steps, to the desired information. Such signals are represented by the absence or presence of fixed voltage levels returned to ground either occurring at the outputs or applied to the inputs of logic gates.

Devices designed to make observations of quantities not sensed directly by humans are termed measuring instruments. An instrument, temperature transducer, functions typically by transforming measured temperature into a voltage output and maintains precisely a one-to-one relation between temperature and voltage.

The work reported here sets out the design and implementation of a temperature measuring system (PRT) which operates by converting the quantity into digital bits, using dual slope integration technique, which represent the measured values.

The dual slope converter integrates the input, V_i for a fixed duration of 2^n clocks and then integrates an internal reference ($-V_r$) until the output, is brought back to zero.

The number N, of clock cycles taken to return the integrator to zero is proportional to V_i averaged over the integration period and this represents the output code.

$$N = 2^n V_i / V\gamma$$

2.0 THEORY OF INSTRUMENT DESIGN

Instruments can be classified as devices to monitor and control processes and operations and carry out engineering analysis. The schematic of a basic measuring instrument system is depicted in Fig.1.

The measuring instrument senses, conditions and processes the signal before presenting the measured value to the observer in a recognisable form.

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Fig. 1. : A Basic Measuring Instrument

S = sensing element, C = signal conditioning element, P = signal processing element. D = Data presentation element.

The generalised model of a system is given by the relation G (Doeblin, 1975),

$$G = \frac{B_0 e^{j(\omega t+\phi)}}{A_0 e^{j\omega t}} \quad \text{.......................................} (1)$$

where ω is the angular frequency and $B_0/A_0 < \phi = M < \phi$ and M = magnitude and ϕ is the phase angle. This can be expressed in series (2) from the where orders of instrument are deduced.

Devices which have their output continuously varying with time, and bearing a fixed relationship to the input are analogue and such measurements may be digitally implemented by converting the quantity to be measured into discrete values before presenting the data in digital form with the following advantages.

i: parallax error is eliminated,
ii. human errors are reduced,
iii. superior accuracy in performance with automatic polarity and range indication facilities such that measurement error is minimised,
iv. the output can be interfaced with the computer, allowing permanent records to be made automatically, and
v. output data are immuned to spurious electromagnetic interference.

These qualities are exploited in this project. The output data which are digital are displayed using either Neon Tubes, liquid crystal displays (LCD), light emitting diodes (LED) or the cathode ray tube (CRT). The LCD is used in this work.

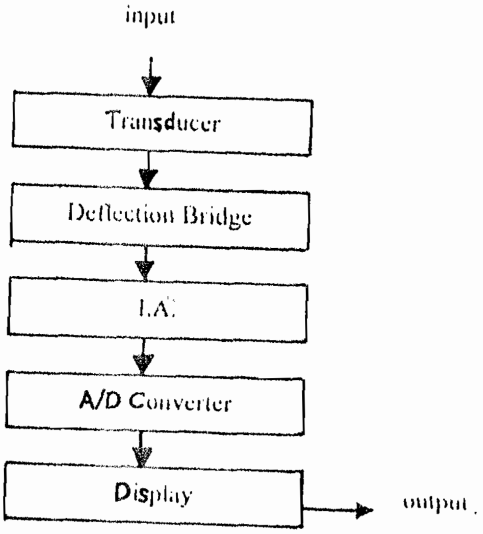

Fig.2 Schematic of a Digital Thermometer.

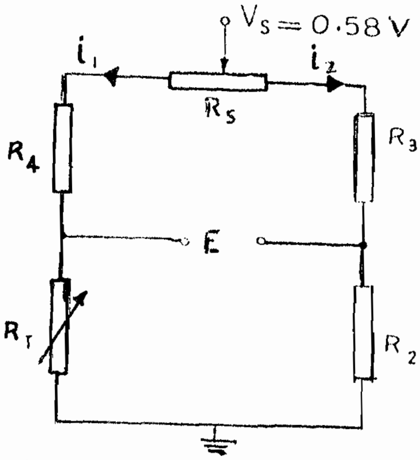

Fig. 3 Deflection bridge circuit

For accurate measurement, instruments have to be stable such that for bounded input, there must be a bounded output (Brook and Wayne, 1991). The stability of instrument systems are determined,

i. from the system transfer function which ensures that all roots of the denominator have negative real parts,
ii. by ensuring that the Nyquist criterion is met,
iii. by is using compensation

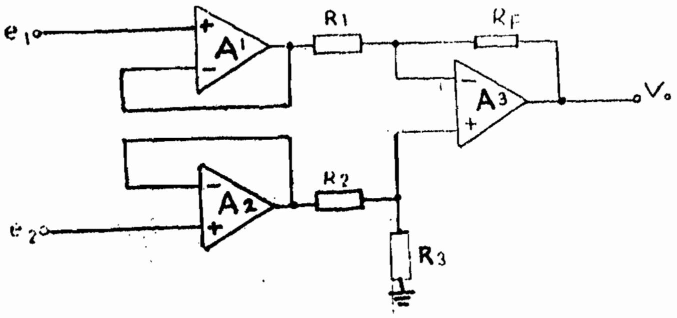

Fig. 4 Instrumentation amplifier circuit

networks (lag, lead or lead-lag),

iv. by applying feedback with reduced but constant loop gain that ensures stability with attendant reduction in noise and distortion and modified input and output impedances.

2.1 DESIGN

Electronic measurement, control and information processing systems consist of an input transducer, a signal modifier and an output.

The schematic of the digital thermometer is in fig.2.

The transducer senses the measurand (temperature) and converts it into electrical signals. A constant current source provides the excitation drive to a wheatstone bridge, which incorporates the transduer, and is operated in the deflection mode. The bridge, initially tuned to produce zero-output indicates the measured input quantity. The signal extracted from the measurand is in the order of mV which is amplified by the instrument amplifier (I.A).

The output signal from the conditioning elements is converted into digital form by the analogue-to-digital (A/D) converter. The display unit receives the A/D converter output and communicates to the human observer. Here, a liquid crystal display (LCD) is used.

2.1.1 PLATINUM RESISTANCE THERMOMETER

The resistance of most materials increases linearly with temperature in the range -100°C - +500°C (Dadoem, 1997). The general relationship between the resistance R_T (ohms) of a metal at temperature T°C is a power series of the form.

$R_T = R_0(1+\alpha T+\beta T^2+\gamma T^3+)$ .... (2)

Where R_0 is the resistance at 0°C and α, β and γ are temperature coefficients of

Table 1: Electronic Switch Positions ICL 7106

State Switch	1	2	3
INPUT	CLOSED	OPEN	OPEN
+REF	OPEN	*	OPEN
-REF	OPEN	*	OPEN
AUTO-ZERO	OPEN	OPEN	CLOSED

+ REF closed for - ve inputs

- REF closed for +ve inputs

Table 2: Results of Test Measurements

				Bridge Output Voltage, $V_0(T)$mV		$\alpha = R/R_0T$
	Temp.°C	R(T)Ω	Δ R(T)Ω	Measured	Calculated	α°C^{-1}
	0.0	1.63	0.00	0.00	0.00	0.00
	30.0	1.81	0.18	1.10	1.64	3.68×10^{-3}
	40.0	1.86	0.23	1.60	2.09	3.53×10^{-3}
	50.0	1.91	0.28	2.00	2.55	3.44×10^{-3}
	60.0	1.96	0.33	2.40	3.00	3.37×10^{-3}
	70.0	2.02	0.39	2.80	3.55	3.42×10^{-3}
	80.0	2.07	0.44	3.30	4.00	3.37×10^{-3}
	90.0	2.13	0.50	3.70	4.54	3.41×10^{-3}
Possible Error	±0.5	±0.01	±0.01	±0.01	±0.01	Average = 3.46×10^{-3}

resistance. Platinum is preferred because it is chemically inert and has linear and repeatable resistance-temperature characteristics and can be used over the range (-200 to 500)°C. In addition, it can be refined to a high degree of purity with small tolerance values and could admit a current less than 5mA (Bentley, 1984) to ensure high accuracy in application.

For the specified range of measurement of this thermometer, 0°C and 200°C, the three standard fixed points of temperature defined for calibrating the thermometer are (i) ice-point 0°C, (ii) steam-point 100°C at 760mmHg and (iii) freezing point of tin –231.97°C at STP.

2.1.2 THE DEFLECTION BRIDGE

To measure resistance deviation, R is converted to voltage variation, V, in the voltage divider circuit of fig.3. It is shown that the bridge circuit can be represented by its thevenin equivalent circuit (Bentley, 1984), with

$$E_{TH} = V_s\left(\frac{R_T}{R_T + R_4} - \frac{R_2}{R_2 + R_3}\right)$$

and

$$R_{TH} = V_s\left(\frac{R_T R_4}{R_T + R_4} + \frac{R_2 R_3}{R_2 + R_3}\right) \;\ldots\ldots\ldots\ldots\ldots (3)$$

The bridge can become unsteady in performance due to resistance tolerance thereby degrading the signal from the sensor. In this design, resistance trimming is used to improve bridge performance and R_5 is employed to null the effect of resistance mismatch.

The sensor employs platinum resistance wire of 1.63ohms at 25°C. With a current of 0.2mA on each side of the bridge ($(R_T + R_4 + R_5)/2 = V_s/2 = 2.9k\Omega$); R_5 compensates for up to 2% variations on each side of the bridge. The power, P dissipated is 0.06mW.

2.1.3 THE INSTRUMENTATION AMPLIFIER

The data amplifier is necessary to step up the weak signal emanating from the sensor. This is made of two sections.

i. The FET input operational amplifiers (O.A), A_1 and A_2 configured as voltage followers provide the desired high input impedance.
ii. The LM 318(OA), connected in the common mode, provides voltage amplification of the signal.

Fig.4 is the instrumentation amplifier circuit where the (OA) A_1 A_2 provide unity gain each are connected as voltage followers; while A_3 is designed to provide a gain of 12 such that:

$V_o = R_f/R_1\,(e_2 - e_1)$ with $R_1 = R_2 = 200k\Omega$ and

$R_3 = R_f = 18k\Omega$.

2.1.4 ANALOGUE-TO-DIGITAL CONVERTER (A/D-C)

The analogue-to-digital converter (A/D-C) employed is the Dual-Slope type, with the following relative merits (Dadoem, 1997).

i. the conversion accuracy is independent of R, C and OA offsets.
ii. The integrating A/D-C offers excellent linearity and resolution as well as zero differential non-linearity.
iii. It provides excellent noise rejection of a.c signals. The 50Hz or 100Hz bridge pickup is averaged during the input integration phase.
iv. The incorporated Dual ramp converters are suited to highly accurate measurements.
v. But it has low conversion rate.

For this work, the ICL 7106 display-oriented version of the time-proven dual-slope integration technique with all the advantages is employed. It contains the analogue and digital active circuitry on a single chip and drives a three and a half digit panel meter with automatic polarity and auto-zero facilities.

The functional description of the simplified schematic shown in fig.5 is presented in ([illegible]).

The Operation of the ICL 7106 is Highlighted Hereunder

Initially, the control logic sets the electronic switches as in Table I. With input applied to the integrator, comprising amplifier (B) resistor R_1 and capacitor C_1 via a buffer amplifier (A). The integrator output ramps positively or negatively depending on input polarity for a period set by the clock oscillator at the end of which state 2 is selected. The comparator C determines which reference is selected and detects the state of zero integrator output. During state 2, counter accumulates clock pulses until integrator reaches zero and changes state when state 3 is selected. Here, the accumulated count and polarity are displayed. C_2 is then connected between the buffer (A) and the short circuited integrator and comparator.

2.4.1.1 DESIGNING WITH ICL 7106

The system is designed to read 200mV full-scale deflection. The clocking mechanism, is achieved by an RC oscillator connected to pins 38, 39 and 40 (fig.6). The oscillator frequency is divided by four before it clocks the decade counters. It is further divided to form the three converter cycle phase: signal integrate (1000 counts), reference de-integrate (0-2000 counts) and the auto-zero phase (1000-3000 counts).

For these readings per second, an oscillator frequency of 48kHz was used. For all ranges of frequency, f, a 100kΩ resistor was used and the capacitor was selected from the equation,

$f = 0.45/(R_3C_4)$.

2.4.1.2 THE INTEGRATOR

R_1 and C, determine the integrator time constant. Both the buffer amplifier and the integrator have class A output stage with 100μA of quiescent current. The integrating resistor selected is large enough to maintain linearity over the input voltage range and for the 200mV scale, 47kΩ is optimum. The integrating capacitor is selected to give maximum voltage swing. For three readings s^1 (48kHz) clock, C_1 = 220nF and C_2 = 47nF. C_2 reduces susceptibility to noise of the auto-zero circuitry and the display is designed to read zero when analogue input is zero.

The R.C filter with R_5 (1MΩ) and C_5 (10nF) introduces an error of less than 1μV which is negligible.

An input attenuator $R_2/(R_1+R_2)$ is incorporated to enable the meter measure in excess of 200mV.

The ICL 7106 input is connected to the output of the instrument amplifier with a V_{re} equal to $V_i/2$ volts.

The component values for the design are:

R_1 = 47k
R_2 = 1k
R_3 = 100k preset
R_4 = 22k
R_5 = 1M

C_1 = 200nF
C_2 = 470nF
C_3 = 100nF
C_4 = 100pF
C_5 = 10nF

All resistors are 5% carbon composition type and capacitors are assorted silver mica.

2.4.1.3 DIGITAL DISPLAY

This unit consists of a digital panel meter module with a 3½ digit LCD incorporating a wide range of commonly employed symbols like mA, k, mV, M, Ω, °C.

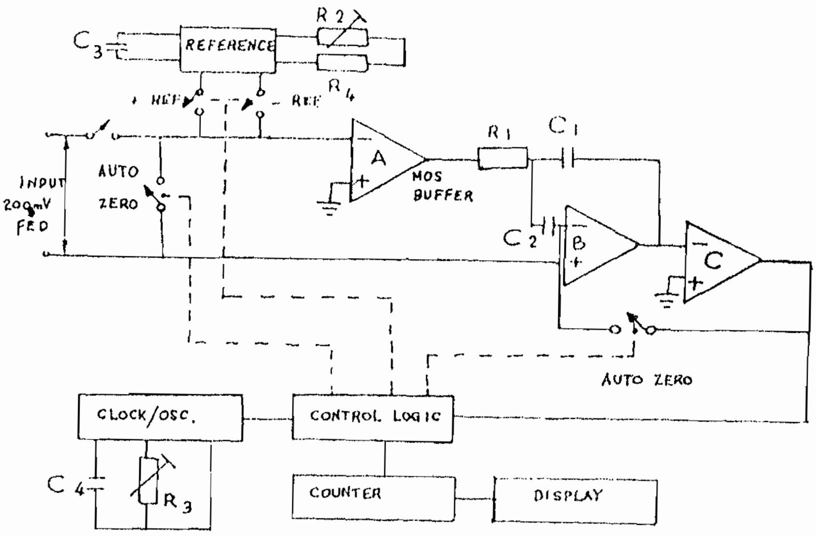

Fig. 5 Schematic diagram of IC L7106 ADC.

This operation of the digital meter is centred around the ICL 7106 IC having matched characteristics. The LCD segments are illuminated by signals emanating from the action of the 4543B BCD-to-7-segment latch/decoder/drivers resident in the ICL 7106 as in fig.6.

3.0 MEASUREMENTS AND ANALYSES

The prototype PRT was set up and test performance carried out. The equipment used to perform the tests and measurements were.

i. a regulated water bath (Tecam TE-7 Tempette)
ii. a mecury-in-glass thermometer, -10 to 200°C x 1°C
iii. a gold precision digital multimeter (mode M225)
iv. a high resolution digital multimeter (Thur/by mod.1503HA)
v. a chart recorder, linear 200 (mod.1202-000).

3.1 CALIBRATION OF THE BRIGDE

The sensor probe was immersed in a funnel of ice-chips maintained at °C and the bridge adjusted for output $V_0 = 0V$. The resistance of the sensor at 0°C was measured using the high resolution digital multimeter.

The water bath was heated to raise the temperature of the sensor. Readings of the output voltage and resistance were taken at intervals of 10°C. The range of temperature covered was however limited to 94°C due to lack of facility to attain high temperatures. Results are given in Table (3). The calibration curve is in fig.7.

To determine α and β, we recall the expression:

$R_T = R_0(1+\alpha T+\beta T^2+\gamma T^3+.....)$...... (3.1)

The resistance of the sensor was measured at the temperatures 0°C, 50°C and 90°C. With resistance values substituted into (3.1), a set of equations were solved to obtain.

$\alpha = 3.47 \times 10^{-3}\ (°C)^{-1}$

and $\beta = 5.82 \times 10^{-7}\ (°C)^{-2}$.

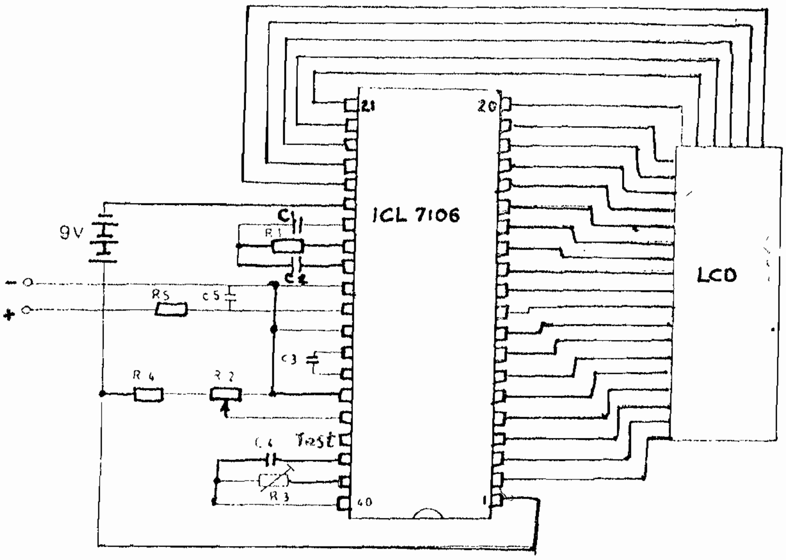

Fig. 6 Pin configuration of ICL7106

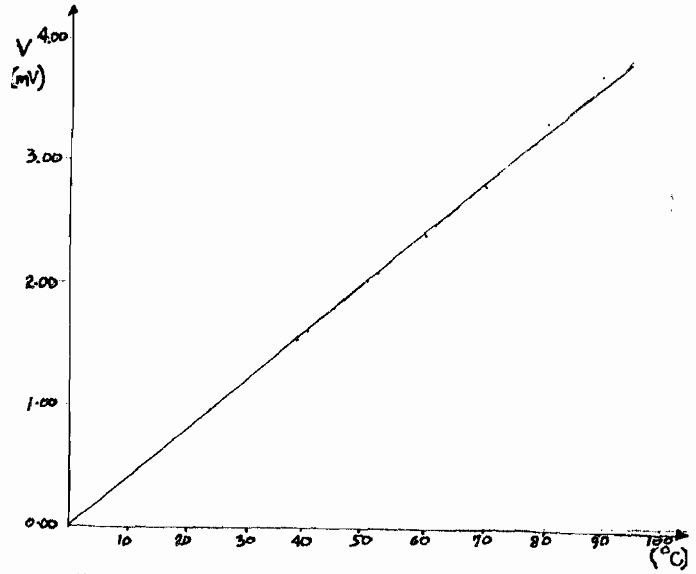

Fig. 7 Calibration curve of the Digital Thermometer

The slope from the calibration curve is determined as 0.0400±0.0018mV°C. Since the graph is linear and of the form y = a + bx, employing the least squares fit, a and b are determined (Dadoem, 1997) and found to be –0.16 and 0.04 respectively such that y = -0.16 + 0.04x and by interpolation and extrapolation, for x = 50°C, y = 1.84mV and for x = 100°C, y = 4.00mV.

3.2 LINEARITY

The manner in which Vo changes with equal steps of temperature change shows

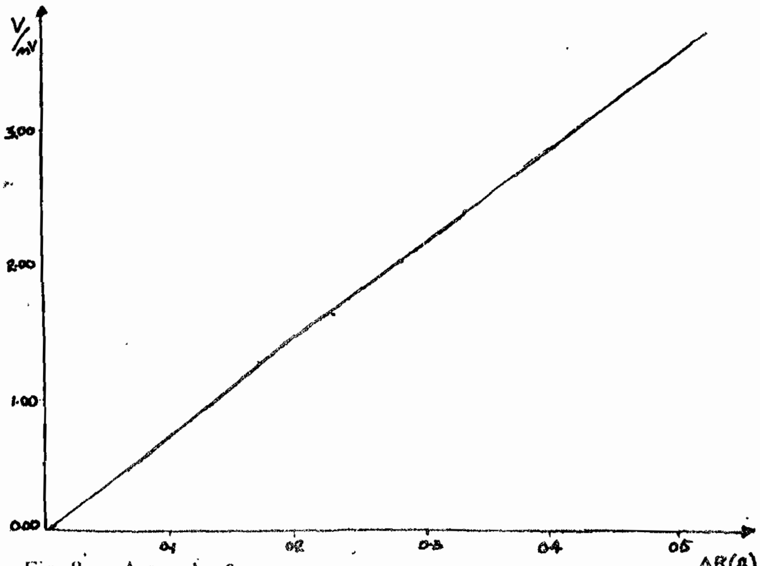

Fig. 8 A graph of output voltage against change in resistance.

slight non-linearity. In this design however, such a problem was reduced.

i. by driving the deflection bridge with a low but constant d.c. excitation voltage of 0.58V.
ii. by carefully selecting the values of the resistive elements in the bridge in order to limit the electrical heating power in the sensor element .

The sensitivity of the bridge is given by the slope of the fig.8 as 0.0400 $\pm 0.0018 mV°C^{-1}$ and the ratio of the resistor values were low enough to maintain the sensitivity and the overall the sensitivity of the system was found to be $7.13 \pm 0.58 mV\Omega^{-1}$ with the power dissipated given as in the sensor is 0.14mW.

3.3 NUMBER PRESENTATION IN BCD AND DECIMAL EQUIVALENTS

The signal digitalization and decimal counting unit are fully described in (Dadoem, 1997). The digital counter consists of four decades in cascade; each having a decade counter, a memory, a BCD-to-denary decoder, the indicator driver and the LCD indicator. The input signal is counted and as soon as the first count goes from 9 back to 0, a carry is presented to the next decade. This thus counts one for every ten input pulses. In the same way, the 'third decade register indicates the hundreds and the fourth, the thousands and so on. When counting is concluded, the various decades become steady and contain the binary coded information.

The status of the respective binary digits then illuminate the appropriate segments of the 7-segment displays.

3.4 ACCURACY OF INSTRUMENT

Design steps taken to enhance performance accuracy in the digital thermometer are as follows:

i. Loading error due to meter drawing current from C.V.T was remedied by making input

Table 3: Results Obtained from the Differential Amplifier

	Temp.°C	Bridge Output Voltage, $V_0(T)$mV	Amplifier Output Voltage, (mV)
	0.0	0.00	0.00
	30.0	1.10	30.03
	40.0	1.60	38.15
	50.0	2.00	46.67
	60.0	2.40	54.90
	70.0	2.80	64.97
	80.0	3.30	73.20
	90.0	3.70	83.08
Possible Error	±0.5	±0.01	±0.01

impedance very high (100MΩ) using FET.

ii. Series mode error caused by a.c. voltage superposed on the d.c signal to be measured was minimized by using integration technique during the averaging process and the input circuit to A/D – C incorporates an RC filter.

ii. Common mode error due to poor regulation of the power supply and RF interference pickup, which result in non-linearity of low level transducer is limited by.
  - using differential amplifiers
  - adequate decoupling and stabilization of supplies
  - maintaining separate analogue and digital ground.

4.0 CONCLUSION

A complete measuring instrument (Digital Thermometer) was designed and implemented using available components. The analogue signal conditioning circuit of the system is made up of sensor (pt. Wire), deflection bridge and instrumentation amplifier. Measurements made produced results in Table 4. Limitation of facilities dictated the range covered.

The digital circuit (using dual-slope technique), was designed to process d.c. signal strength in the range 0-200mV f.s.d. Two levels of d.c. power supply were employed for the analogue and digital circuits. While the analogue circuit was energized by ±15V from a stabilized power supply unit, the digital circuit was powered using a 9V battery (PP3).

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