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TEMPERATURE VARIATION EFFECTS ON CARBON NANOTUBE FIELD EFFECT TRANSISTOR (CNTFET) BASED ON SIMULATION STUDY

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ABSTRACT
Carbon Nanotube Field Effect Transistors (CNTFET) are promising Nano-scaled devices for implementing high performance and low power circuits. As the conventional silicon metal-oxide-semiconductor field-effect transistor (MOSFET) approaches its scaling limits, many novel device structures are being extensively explored. The CNTs give a great opportunity of scaling the circuit design to the Nano regime. The aim of this research work is to study the temperature variation effects in carbon nanotube FET based on simulation study. A Nano device simulator called FETtoy was used to study the temperature variation effect, CNTFETs as channel materials with TiO_2 as dielectric materials and gate control parameter 0.88. The scope of this research work covered low temperature range to high temperature range (273 K to 375 K) with other parameters such as; diameter of CNT (carbon nanotube), drain control and transport effective mass fixed. The various output parameters that were studied are drain current versus gate voltage, quantum capacitor versus gate voltage, drain induced barrier lowering (DIBL), threshold swing (S), On current (I_{on}), Off current (I_{off}), transconductance (g_m), output conductance (g_d), carrier injection velocity (v_{inj}), and Voltage gain (A_v). From the results obtained, carbon nanotube as channel material with TiO_2, gate control 0.88 at room temperature (300 K) can be used to suppress the subthreshold effects in nanodevices.
KEYWORDS: Ballistic nanoscale MOSFET, Channel materials, FETtoy simulating software, Short channel effects (SCEs), Drain Induces Barrier Lowering (DIBL)

INTRODUCTION

In the growing era of nanotechnology, the electronic devices are moving fast towards the nanotechnology. As the conventional silicon MOSFET scaling approaches its scaling limit, new device structures are being investigated and explored (Ganesh *et al.,* 2010). Among them, carbon nanotube has captured almost every sphere of the technological aspect of electronic devices (Mitali and Rajesh, 2017). The essential physics of carbon nanotube transistors are electrostatics, ballistic transport and band gap (Alokik, 2003). Gordon Moore made the very important observation that the number of components on minimum cost integrated circuits had increased roughly by a factor of two per year which then later transformed itself into a law known as the Moore's Law (Moore, 1965). As the MOSFET gate length enters the nanometer regime, however, high power dissipation, high leakage current, short channel effects (SCEs) (Taur and Ming, 1998) such as threshold voltage (V_{th}) roll off and drain-induced-barrier-lowering (DIBL), become increasingly significant, which limits the scaling capability of planar bulk or silicon-on-insulator (SOI) MOSFETs (Galadanci, *et al.,* 2017b). At the same time, the relatively low carrier mobility in silicon (compared with other semiconductors) may also degrade the MOSFET device performance (Meishoku *et al.,* 2001).

Various novel device structures and materials like carbon nanotube transistors (Cui *et al.,* 2003); Wang *et al.*, (2003); Javery *et al.* (2003) molecular transistors, the effect of gate length on the operation of silicon-on insulator (SOI) MOSFET structure, using three transistors with gate lengths of 100, 200 and 500 nm with a fixed channel length of 500nm were simulated and when the gate length is increased the output drain current and the transistor transconductance increases (Arabshahi Baedia,

(2010), the effect of gate length on DG-MOSFET at Nano regime was studied, where by DG-MOSFETs with gate lengths of 20,40, 60, 80 and 100nm were simulated respectively with a fixed channel length of 100nm, oxide thickness of 1.0nm and channel thickness of 3nm, using simulation software Nano-FET (Galadanci *et al.,* 2017a), performance analysis of electrical characteristics of single gate and double gate Nano-MOSFET devices using FETTOYsimulating software (Galadanci *et al.,* 2018) are being extensively explored.

In this work, the effects of temperature variation in carbon nanotube as channel material was analyzed using Nano electronics device simulating software's (FETTOY and Nano-MOS 2.5) to study the electrical properties. The electrical properties considered are drain current versus gate voltage, quantum capacitance versus gate voltage, drain induced barrier lowering (DIBL), threshold swing, on – off current, transconductance, output conductance, voltage gain and carrier injection velocity with TiO_2 as dielectric materials and other parameters fixed.

STRUCTURE CARBON NANOTUBE

A Carbon Nanotube Field Effect Transistors (CNTFET) are promising nano-scaled devices for implementing high performance very dense and low power circuits. A Carbon Nanotube Field Effect Transistor refers to a FET that utilizes a single CNT or an array of CNT's as the channel material instead of bulk silicon in the traditional MOSFET structure (Martel *et al.,* 1998). The core of a CNTFET is a carbon nanotube which was discovered (Ijiima, 1991) with a typical diameter of 1-20nm they can reach a length of millimeters (Hang *et al.,* 2003).

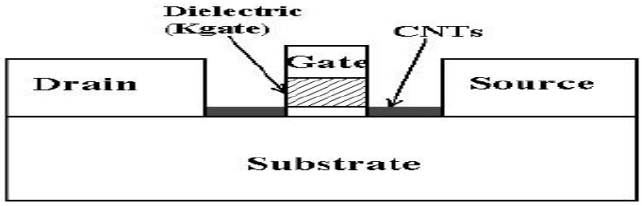

Figure 1: Carbon nanotube FET [14].

Carbon nanotube MOSFET model

An applied gate voltage $V_g$will induce charge carriers in the nanotube that can contribute to a current passing the nanotube (NT). The induced charge density might not linearly depend on the gate voltage. The surface potential which corresponds to the Fermi energy in case of nanotubes can be related to the applied voltage. For this reason, the Fermi energy estimated within the CNT when a gate voltage V_g is applied. The number of induced carriers can be calculated from the Fermi energy and finally estimate the conductance G as function of the back–gate voltage V_g.

In analogy to the MOSFET theory where the MOS capacitance is studied at the silicon-oxide-CNT structure. The capacitance $C = dQ/dV$ of this structure is best described by the model of a thin metallic wire at distance d from an infinitely large metallic plate (Wunnicke, 2006).

If the radius of the wire r is much smaller than the distance to the metal plate $r \ll d$, a simple solution can be given for the capacitance per unit length $C_{ox}^{*} = \frac{C_{ox}}{L}$ (Wunnicke, 2006), this implies that;

$$C_{ox}^{*} = \frac{2\pi\varepsilon_o\varepsilon_r}{In(\frac{2d}{r}+2)} \qquad (1)$$

The nanotube is not surrounded by one single gate dielectric. Between the gate and the nanotube there is SiO_2 with $\varepsilon_{SiO_2} \approx 3.9$, whereas above is air with $\varepsilon_{air} \approx 1$. This as to be considered by an effective dielectric constant $\varepsilon_r^{eff} \sim \frac{\varepsilon_{SiO_2}}{2} \sim 2$ as shown in (Wunnicke, 2006; Vashaee *et al.,* 2006). With an oxide spacing of $d = 400nm$ and a tube radius of $r = 2nm$ to $C_{ox}^{*} \sim 20pF/m$.

Subthreshold regime

In depletion, the small mobile charge that can be thermally excited in the depletion zone gives rise to a small subthreshold current. The carrier concentration is far away from the Fermi energy given by the Boltzmann distribution $n = n_i \exp(^{-e\Psi}/_{kT})$ and so.

$$Q = e\int_0^{W_d} n(x)dx = e\int_{\Psi_s}^{0} \frac{n(\Psi)}{d\Psi/\mathrm{dx}} d\Psi =$$

$$en_i \int_{\Psi_s}^{0} \frac{1}{d\Psi/\mathrm{dx}} \exp(^{-e\Psi}/_{kT}) d\Psi \qquad (2)$$

The integral approximately is given by [19];

$$Q = KT\sqrt{\frac{\varepsilon_{Si}\varepsilon_o}{2e\Psi_s N_a}}\left(\frac{n_i}{N_a}\right)^2 \exp\left(^{-e\Psi}/_{kT}\right) \qquad (3)$$

The mobile charge in the depletion region and the current in the subthreshold regime depend

exponentially on the surface potential Ψ_s: $I \propto \exp\left(-e\Psi/kT\right)$.

$$S = \left|\frac{dV_g}{d(\log(I))}\right| = \left|In(10)\frac{dV_g}{d(\ln(I))}\right| = In(10)\frac{dV_g}{e/kTd\Psi_s} \quad (4)$$

$$S = 59.6mV\frac{kT}{e}\left(1+\frac{C_d}{C_{ox}}\right) \quad (5)$$

Quantum capacitance

Quantum capacitance (CQ) is associated with the properties of channel material. The quantum capacitance was first introduced by Luryi (1998). It is defined as the derivative of total net charge of device with respect to electrostatic potential. The total charge is proportional to the weighted average of the density of states at the Fermi level ÆF. When the density of states as a function of energy is known, the quantum capacitance CQ of the channel materials can be calculated as Datta (2005).

$$C_Q = e^2\int_{-\infty}^{+\infty} f(E)\left(-\frac{\partial f(E-E_F)}{\partial E}\right)dE \quad (6)$$

The insulator capacitance is inversely proportional to the insulator thickness. Ideally the inversion layer capacitance is much larger than the insulator capacitance in the strong inversion condition and gate capacitance approaches the insulator capacitance.

In a truly ballistic transistor, the on-current per unit device width (*Ion*) is given by the inversion density *Ninv* times the average injection velocity *vinj* at the virtual source.

Ion is given in terms of technological and channel material parameters by the following Expression (Rakesh and Devi, 2013):

$$I_{on} = \frac{8qh}{3\sqrt{\pi}}\frac{(N_{inv})^{\frac{3}{2}}}{(n_v)^{\frac{1}{2}}(m_w)^{\frac{1}{4}}(m_L)^{\frac{3}{4}}} \quad (7)$$

where *nv* is the valley degeneracy, while *mL* and *mw* are the effective masses in the direction of

The subthreshold swing (S) is defined as the gate voltage charge needed to suppress the subthreshold current (Taylor, 1978).

the channel length and width, respectively. The expression given in (7) suggests that the maximum *Ion* is obtained for the smallest transport masses and valley degeneracy.

MATERIALS AND METHODS

The list and details of materials used and the method employed in this study are presented in this part.

Materials

The materials used in this work are: Zinox Computer rating 3.3 windows experience index, with Dual-core processor 2.30GHz, 2.00GB installed RAM and 32-Bits operating system, FETtoy simulating software.

Method

To analyze the ballistic transport properties of carbon nanotube, the simulation and modeling was achieved through FETtoy simulators as shown in Figure 2. FETTOY tool is a numerical simulator that calculates the ballistic I-V characteristics for a conventional carbon nanotube MOSFET. FETTOY assumes a nanotube MOSFETs as cylindrical geometry (Natori, 1994). However, in the simulation, the device type selected is carbon nanotube as channel material, silicon as the substrate body, oxide thickness of 0.3nm, initial source fermi level (eV) -0.320, drain control 0.035 and transport effective mass 0.19

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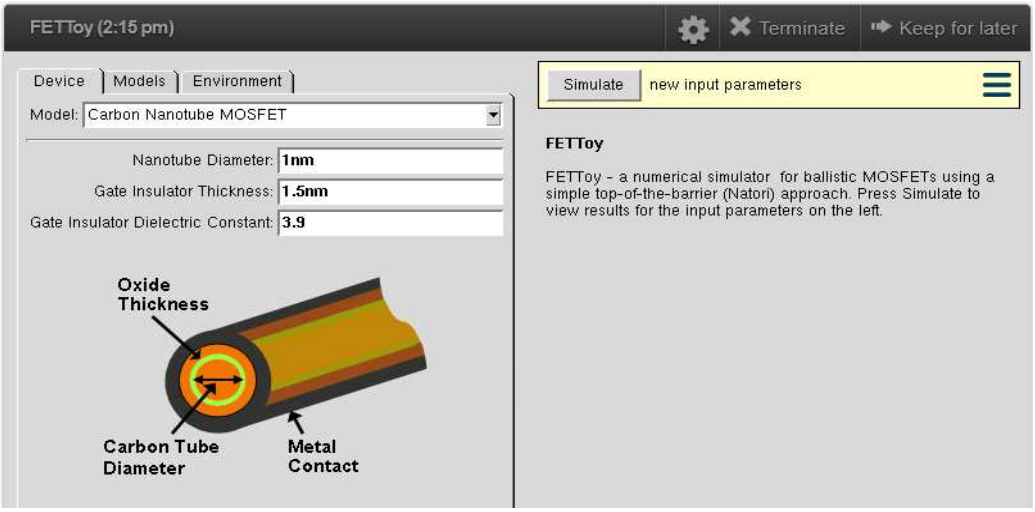

Figure 2: FETTOY Software interface for carbon nanotube MOSFET

The simulating procedure was as follows;

1. Modelling of the device was done by choosing the device type (carbon nanotube)
2. Setting the value of temperature for sets of values (273 K, 300 K, 325 K, 350 K, 375 K) with TiO_2as dielectric material, gate control parameter 0.88 and diameter of CNT 1.0 nm.
3. The program is then run to obtain results for each set of temperature chosen.
4. The results of drain current and quantum capacitance were obtained and analyzed for different dielectric materials, variation of gate control parameter and temperature.

We studied the simulation for different temperature rangeswith TiO_2 as dielectric material, oxide thickness 0.3nm and the gate control parameter 0.88. Table 1 consists of input parameters for the FETTOY simulators (set of MATLAB programs for simulating the carbon nanotube field effect transistors).

Table 1: Values of Input Parameters

FETTOY INPUT PARAMETERS	**VALUES**
Oxide Thickness	0.3 (nm)
Insulator dielectric constant	40
Temperature	273-375 (K)
Initial gate voltage	0 (V)
Final gate voltage	1 (V)
Number of bias points (gate)	13
Initial drain voltage	0 (V)
Final drain voltage	1 (V)
Number of bias points (drain)	13
threshold voltage	0.32
Gate control parameter	0.88
Drain control parameter	0.035
Series Resistance	0 (ohms)
Doping Density	1e+26 (/m^3)
Si Body Thickness	1e-08 (m)
Transport Effective Mass	0.19
Valley Degeneracy	2
Diameter	1.0nm

RESULTS AND DISCUSSION

The simulation results of carbon nanotube FET obtained are drain current versus gate voltage $(I_d - V_g)$, quantum capacitance versus gate voltage $(C_Q - V_g)$, drain induced barrier lowering (DIBL), threshold swing, on – off current, transconductance, output conductance, voltage gain and carrier injection velocity for different dielectric materials, variation in gate control parameters and temperature. At low gate voltages, the transistor is in its off state and very little current flows in response to a drain voltage V_d. Beyond a certain gate voltage, called the threshold voltage V_{th}, the transistor is turned on and the ON-current increases with increasing gate voltage V_g.

Drain current (I_d) against gate voltage (V_g)

Figures3 and 4, show (I_d) vs (V_g) of CNTFET and SNWFET at different temperatures. There is no appreciable variation for change in temperature in both CNTFET and SNWFET by Raja *et al.* (2012). At room temperature, CNTFET has higher drain current around 59.8 micro amps with higher gate voltage 1.0 volts which is very similar or the same when comparing with other temperature curves.

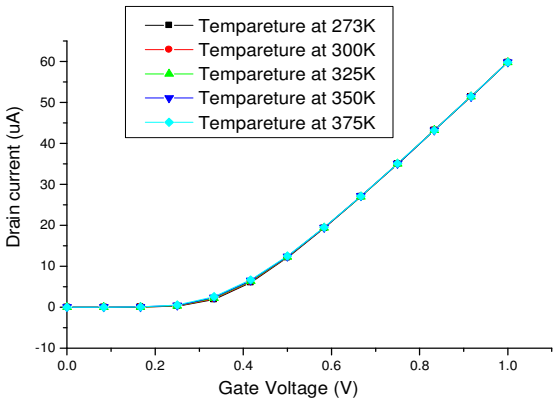

Figure 3: I_d-V_g for different temperature of Carbon nanotubeFET

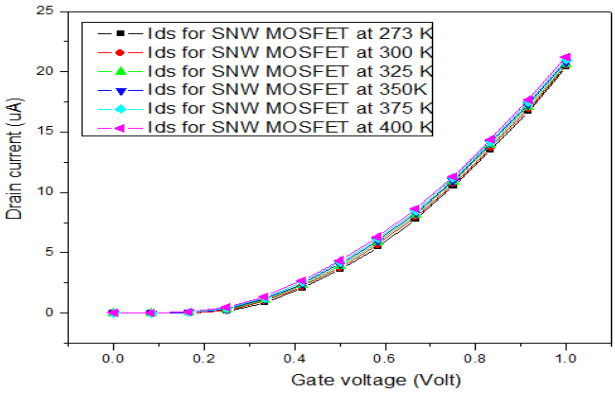

Figure 4: I_d-V_g for different temperature of Silicon nanowire FET [24]

Quantum capacitance C_Q versus gate voltage $V_g(C_Q - V_g)$characteristics

Simulations were carried out to obtain $C_Q - V_g$ in a carbon nanotube FET with drain voltage as 1V and variations in input parameters. Quantum capacitance C_Q is associated with the properties of channel material which was first introduced by [20]. The quantum capacitance C_Q plays significant role in comparing with gate oxide capacitance Cg. When Cg is much greater than C_Q, it can be shown that the device can be operated near to Quantum Capacitance Limit. When the device is in quantum confinement limit, $C_Q - V_g$ curves at full degenerate (high gate bias) and no degenerate (low gate bias limits) are investigated (Ganesh *et al.,* 2010). Figure 5 and 6, shows the C_Q-V_g curves at different temperatures. As the gate voltage increases up to 0.583 volt, the quantum capacitance decreases with increase in temperature. At room temperature Quantum capacitance value at higher voltage is 1.88pf full degeneration which is the same for all other temperature curves

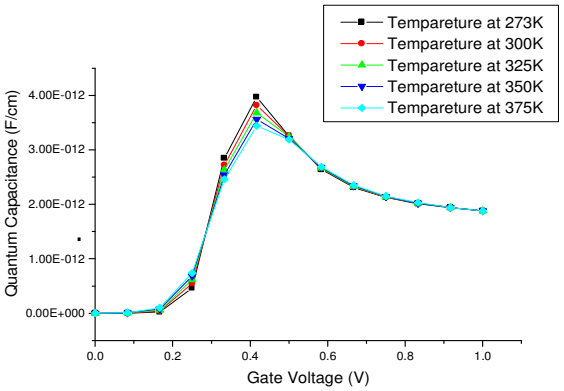

Figure 5: C_Q-V_g for different temperature of Carbon nanotube FET

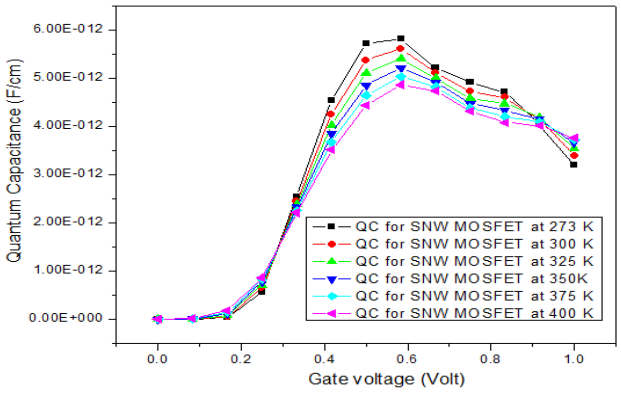

Figure 6: C_Q-V_g for different gate temperature of Silicon nanowire FET [24].

Sub Threshold Parameters on Variation of Temperature

The devices sub threshold regions are drain induced barrier lowering (DIBL), threshold swing, on – off current, transconductance, output conductance, voltage gain and carrier injection velocity. Device physics and design equations of carbon nanotube transistors are given in detail in [3; 9]. Table 2, is the carbon nanotube transistor output values using FETtoy which shows the simulation result on variation of temperatures in the results. We notice that an increase in temperature leads to a very small significant increase in I_{ON}, or drive current, transconductance, carries injection velocity, output conductance, voltage gain, DIBL and threshold swing. In addition, the off current I_{OFF} when the temperature is at 273 K and 300 K is small, which means the power being wasted while the transistor is off is greatly reduced.

Table 2: Output result of Carbon Nanotube FET using different Temperature ranges

Output parameters	CNTFET with Temperature (273) K	CNTFET with Temperature (300) K	CNTFET with Temperature (325) K	CNTFET with Temperature (350) K	CNTFET with Temperature (375) K
Ion (A)	5.978e-05	5.979e-05	5.979e-05	5.979e-05	5.980e-05
Ioff (A)	2.024e-11	6.611e-11	1.671e-10	3.720e-10	7.479e-10
Threshold swing (S) mV/dec	61.72	67.79	73.44	79.13	84.85
DIBL mV/V	36.88	39.67	40.97	41.92	42.81
Trans conductance (gm) S/m	1.002e-04	1.002e-04	1.001e-04	1.001e-04	1.001e-04
Output conductance (gd) S/m	3.999e-06	3.999e-06	3.998e-06	3.997e-06	3.997e-06
Voltage gain at highest gate & drain Bias (Av)	25.05	25.05	25.05	25.05	25.05
Carries injection velocity (v_inj) m/s	5.434e+05	5.434e+05	5.435e+05	5.437e+05	5.438e+05
Ion/Ioff ratio	2.95E+06	9.04E+05	3.58E+05	1.61E+05	8.00E+04

CONCLUSION

In this work, temperature variation effects on carbon nanotube field effect transistor were analyzed using Nano electronics device simulating software. The device metrics considered are drain current versus gate voltage, quantum capacitance versus gate voltage, drain induced barrier lowering (DIBL), threshold swing, on – off current, transconductance, output conductance, voltage gain and carrier injection velocity with different temperature ranges. From the results obtained, there is no appreciable variation for change in temperature. At room temperature, CNTFET has higher drain current around 59.8 micro amps and the quantum capacitance value at higher voltage is 1.88pf full degeneration which is the same for all other temperature curves.

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