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COMPARATIVE STUDY OF ELECTRICAL PROPERTIES OF CARBON NANO TUBE (CNT) AND SILICON NANOWIRE (SNW) MOSFET DEVICES

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ABSTRACT
Metal oxide semiconductor field effect transistor (MOSFET) is a semiconductor device used in many electronic devices for amplification and switching electrical signals. MOSFET downscaling has been the driving force towards the technological advancement, but continuous scaling down of MOSFET causes problem of high power dissipation, high leakage current, Short Channel Effects (SCEs), excessive process variation and reliability issues. In this work, comparative study of electrical properties of carbon nanotube (CNT) and silicon nanowire (SWN) were carried out using CNT and SNW as channel materials, silicon dioxide as the gate dielectric, silicon substrate as base material. The analysis is carried out using FETTOY simulating software for oxide thickness (0.3, 0.5,0.7,0.9 and 1.2nm). The results show that carbon nanotube channel material have highest transconductance (g_m) ***of*** $1.00 \times 10^{-4} S$, ***highest conductance*** (g_d) ***of*** $4.00 \times 10^{-6} S$, ***highest carrier injection velocity*** (v_{inj}) ***of*** $5.43 \times 10^5 m/s$, ***highest on current (Ion) of 59.79*** μA, ***at oxide thickness of 0.3nm when used as MOSFET device and improved short channel effects with subthreshold swing (S) of 67.79 mV/dec and drain induced barrier lowering (DIBL) of 39.67. More results such as drain current*** (I_d) ***versus gate voltage*** (V_g), ***quantum capacitance (QC) versus gate voltage*** (V_g), ***and average velocity of mobile electron versus gate voltage*** (V_g) ***for all devices are also investigated. Various results obtained indicate that CNT has the higher performance of decreasing gate capacitance with decrease in oxide thickness*** (T_{0x}) ***in deep nanometer regime. This decrease in gate capacitance is observed at a gate voltage of 0.5V and above which leads to the reduction of propagation delay, lower leakage current, low power dissipation, short channel effects (SCEs) as compared to silicon nanowire MOSFET device.***
KEYWORDS: Ballistic nanoscale MOSFET, Channel materials, FETTOY simulating software, Short channel effects (SCEs), Drain Induces Barrier Lowering (DIBL)

INTRODUCTION

Shrinking of the device dimensions is the driving force towards circuit miniaturization, portability and low cost (Sanjeet and Suarabh, 2013). As the device dimensions are getting smaller and smaller, scaling the silicon based MOSFET devices for barrier potential, threshold voltage, oxide thickness, critical electric field etc. are becoming increasingly harder (Sanjeet and Suarabh, 2013). Further scaling down of MOSFET causes problem of high power dissipation, high leakage current, Short Channel Effects (SCEs), excessive process variation and reliability issues. Many solutions are proposed to overcome these problems. Some of the solutions include modifications on the existing structures and technologies with a hope of extending their scalability, while other solutions encompass the use of new materials and technologies to replace the existing silicon MOSFETS (Sanjeet and Suarabh, 2013).

Many works have been done on transistor miniaturization, Galadanci et al. (2017a), conclude that as transistor decreased in size, the thickness of the gate dielectric has steadily been decreased to increase the gate capacitance and drain current, thereby improving reliability, raising device performance and reducing power dissipation. Prasher et al. (2013), In this interesting journey of transistor size reduction, single gate MOSFET is expected to exhibit a problem of short channel effects (SCE) which will lead to less scaling capabilities. Harsh (2015), studies on the effects of gate length and oxide thickness on DG-MOSFET and concluded that the short channel effect (SCEs) in DG-MOSFET is reduced and thinner gate oxide are necessary for higher drain current. Arabshahi and Baedia (2010), study the effect of gate length on the operation of silicon-on insulator (SOI) MOSFET structure, using three transistors with gate lengths of 100, 200 and 500 nm with a fixed channel length of 500nm were simulated and when the gate length is increased the output drain current and the transistor transconductance increases.

Galadanci et al. (2017b), studied the effect of gate length on DG-MOSFET at nano regime with gate lengths of 20,40, 60, 80 and 100nm were simulated respectively with a fixed channel length of 100nm, oxide thickness of 1.0nm and channel thickness of 3nm, using simulation software nanoFET. Prasher et al. (2013), A double gate (DG) MOSFET which comprises of conducting channel surrounded by gate electrodes on either side offers distinct advantage for scaling and will have improved gate-channel control for reduction of short-channel effects (SCEs). DG-MOSFET has higher drive current and transconductance, lower leakage current thus better scaling capability when compared to the bulk MOSFET by Pradhan et al. (2013). Hu (1996), proposed gate oxide with high-k materials in the oxide region to suppress the gate leakage current with continuous thinning of gate oxide layer but this alternative is yet to demonstrate performance that is superior to planar MOSFET (Pradhan et al. 2013 and Hu 1996). Galadanci et al. (2018), carriedout the performance analysis of electrical characteristics of single gate and double gate nano-MOSFET devices using FETTOY simulating software by varying the oxide thickness (0.3, 0.5, 0.7, 0.9 and 1.2nm), gate voltage 0 – 1 V, constant drain voltage 1V and it was concluded that double gate nano-MOSFET has advanges over single gate in nanometer regime due to high conductivity to reduce leakage current and short channel effects.

In this work, comparative study of electrical properties of carbon nanotube and silicon nanowire MOSFET devices are investigated using FETTOY simulating software at room temperature (RT) by replacing the channel material with carbon nanotube and silicon nanowire. The oxide thickness was varying for sets of value (0.3, 0.5, 0.7, 0.9 and 1.2nm) in accordance to international technology roadmap for semiconductors ITRS (2015) in investigating drain current, quantum capacitance and average velocity of mobile electron for carbon nanotube and silicon nanowire MOSFET devices via simulation with nanoelectronics device simulation software FETTOY.

STRUCTURE OF CNT AND SNW MOSFET DEVICES

The traditional metal–oxide–semiconductor (MOS) structure is obtained by growing a layer of silicon dioxide (SiO2) on top of a silicon substrate and depositing a layer of metal or polycrystalline silicon.

Carbon Nanotube

A Carbon Nanotube Field Effect Transistors (CNTFET) are promising nano-scaled devices for implementing high performance very dense and low power circuits. A Carbon Nanotube Field Effect Transistor refers to a FET that utilizes a single CNT or an array of CNT's as the channel material instead of bulk silicon in the traditional MOSFET structure (Martel et al., 1998). The core of a CNTFET is a carbon nanotube which was discovered (Ijiima, 1991) with a typical diameter of 1-20nm they can reach a length of millimeters (Hang et al., 2003).

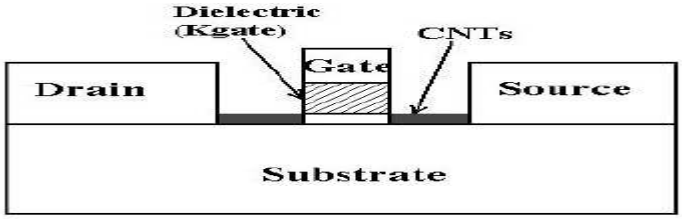

Figure 1: Carbon nanotube FET

Carbon nanotube MOSFET model

An applied gate voltage V_g will induce charge carriers in the nanotube that can contribute to a current passing the nanotube (NT). The induced charge density might not linearly depend on the gate voltage. But the surface potential which corresponds to the Fermi energy in case of nanotubes can be related to the applied voltage. For this reason, the Fermi energy estimated within the CNT when a gate voltage V_g is applied. The number of induced carriers can be calculated from the Fermi energy and finally estimate the conductance G as function of the back–gate voltage V_g.

In analogy to the MOSFET theory where the MOS capacitance is studied at the silicon-oxide-CNT structure. The capacitance $C = dQ/dV$ of this structure is best described by the model of a thin metallic wire at distance d from an infinitely large metallic plate (Wunnicke, 2006).

If the radius of the wire r is much smaller than the distance to the metal plate $r \ll d$, a simple solution can be given for the capacitance per unit length $C_{ox}^{*} = C_{ox}/L$, this implies that;

$$C_{ox}^{*} = \frac{2\pi\varepsilon_o\varepsilon_r}{In(\frac{2d}{r}+2)} \quad (4)$$

The nanotube is not surrounded by one single gate dielectric. Between the gate and the nanotube there is SiO_2 with $\varepsilon_{SiO_2} \approx 3.9$, whereas above is air with $\varepsilon_{air} \approx 1$. This as to be considered by an effective dielectric constant $\varepsilon_r^{eff} \sim \frac{\varepsilon_{SiO_2}}{2} \sim 2$ as show in (Wunnicke, 2006 & Vashaee et al., 2006). With an oxide spacing of $d = 400nm$ and a tube radius of $r = 2nm$ to $C_{ox}^{*} \sim 20pF/m$.

SILICON NANOWIRE FET

A semiconductor nanowire are single crystal structures with a diameter of nano-meters showing interesting and new properties because of their 1D feature and confinement. The nanowire approach to nanoscale MOSFET fabrication offers the possibility for ultimate scaling of the MOSFET. The silicon nanowire FET is modelled with a gate wrapped around the nanowire, this will ensure optimum control of the nanowire potential by the gate potential. This makes nanowires an exceptional choice for the ultimate silicon metal insulator semiconductor (MIS) devices (Galadanci *et al.*, 2017a).

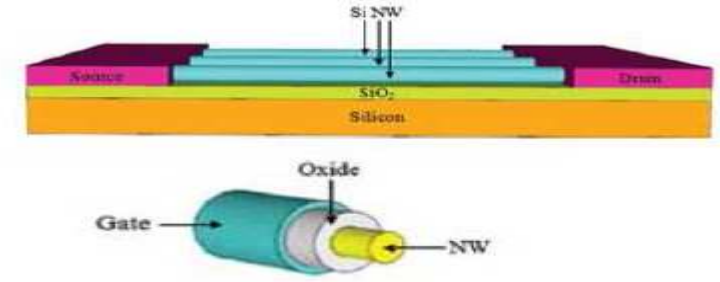

Figure 2: Silicon Nanowire Field Effect Transistor

Silicon nanowire MOSFET model

In CMOS technology down-scaling is driven by the need of ever higher integration. The channel length L is pushed down further and further and with it the gate oxide thickness, applied voltages and device resistance. In contrast to this the channel length L of nanowire FETs and nanowire like structures is much larger than the channel width W Short channel effects (SCEs) don't come into play as the gate insulator thickness d is smaller than the channel length L. But the diameter of the nanowire semiconductor body is now much smaller than the depletion width.

As the semiconductor body is too thin, the last term cannot be related to the depletion capacitance as we used to do for the standard MOS structure. We use the general expression for the relation between the semiconductor charge and the surface potential given by $\frac{dQ_s}{d\Psi_s} = \frac{Aedn}{d\Psi_s} = C_s$ with this relation,

$$\frac{dV_g}{d\Psi_s} = 1 + \frac{C_s(\Psi_s)}{C_{ox}} \quad (5)$$

The gate voltage directly controls the charge in the semiconductor as described in the standard MOSFET theory. In a standard MOSFET the oxide thickness d is much larger than the inversion layer width W_{inv}. In the case of $C_{ox} \gg C_s$ equation (5) simplifier to $V_g = \Psi_s + constant.$ The gate voltage directly controls the surface potential Ψ_s of the semiconductor (Lundstrom & Guo, 2006).

In a semiconductor any local charge is screened within the so-called De-bye screening length range of $L_D = 40nm$ for $n = 10^6 cm^{-3}$ (Sze & NG, 2007).

$$L_D = \sqrt{\frac{kT\varepsilon_{Si}\varepsilon_o}{ne^2}} \quad (6)$$

SUBTHRESHOLD REGIME

In depletion, the small mobile charge that can be thermally excited in the depletion zone gives rise to a small subthreshold current. The carrier concentration is far away from the Fermi energy is given by the Boltzmann distribution $n = n_i \exp\left(-e\Psi/kT\right)$ and so.

$Q = e\int_0^{W_d} n(x)dx = e\Psi s0n(\Psi)d\Psi/\mathrm{d}x d\Psi = \mathrm{e}n\Psi s01d\Psi/\mathrm{d}x\exp\left(-e\Psi kT\right)d\Psi$ (7)

The integral approximatively is given by (Taylor, 1978);

$$Q = KT\sqrt{\frac{\varepsilon_{Si}\varepsilon_o}{2e\Psi_s N_a}}\left(\frac{n_i}{N_a}\right)^2 \exp\left(-e\Psi/kT\right) \quad (8)$$

The mobile charge in the depletion region and the current in the subthreshold regime depend exponentially on the surface potential Ψ_s: $I \propto \exp\left(-e\Psi/kT\right)$.

The subthreshold swing (S) is defined as the gate voltage charge needed to suppress the subthreshold current (Taylor, 1978).

$$S = \left|\frac{dV_g}{d(\log(I))}\right| = \left|In(10)\frac{dV_g}{d(\ln(I))}\right| = In(10)\frac{dV_g}{e/kTd\Psi_s} \quad (22)$$

$$S = 59.6mV\frac{kT}{e}\left(1+\frac{C_d}{C_{ox}}\right) \quad (9)$$

Quantum Capacitance

Quantum capacitance (CQ) is associated with the properties of channel material. The quantum capacitance was first introduced by (Luryi, 1998). It is defined as the derivative of total net charge of device with respect to electrostatic potential. The total charge is proportional to the weighted average of the density of states at the Fermi level *E*F. When the density of states as a function of energy is known, the quantum capacitance CQ of the channel materials can be calculated as (Datta, 2005).

$$C_Q = e^2\int_{-\infty}^{+\infty} f(E)\left(-\frac{\partial f(E-E_F)}{\partial E}\right)dE \quad (10)$$

The insulator capacitance is inversely proportional to the insulator thickness. Ideally the inversion layer capacitance is much larger than the insulator capacitance in the strong inversion condition and gate capacitance approaches the insulator capacitance.

In a truly ballistic transistor, the on-current per unit device width (*Ion*) is given by the inversion density *Ninv* times the average injection velocity *vinj* at the virtual source. *Ion* is given in terms of technological and channel material parameters by the following expression:

Ion is given in terms of technological and channel material parameters by the following Expression (Rakesh, 2013):

$$I_{on} = \frac{8qh}{3\sqrt{\pi}}\frac{(N_{inv})^{\frac{3}{2}}}{(n_v)^{\frac{1}{2}}(m_w)^{\frac{1}{4}}(m_L)^{\frac{3}{4}}} \quad (11)$$

where *nv* is the valley degeneracy, while *mL* and *mw* are the effective masses in the direction of the channel length and width, respectively. The expression given in (11) suggests that the maximum *Ion* is obtained for the smallest transport masses and valley degeneracy.

Method Of Simulation

To analyze the ballistic transport properties of carbon nanotube and silicon nanowire MOSFET, the simulation and modeling was achieved through FETTOY. FETTOY tool is a numerical simulator that calculate the ballistic I-V characteristics for a conventional carbon nanotube and silicon nanowire MOSFET. For conventional MOSFET, FETTOY assumes nanowire and nanotube MOSFETs as cylindrical geometry (Natori, 1994).

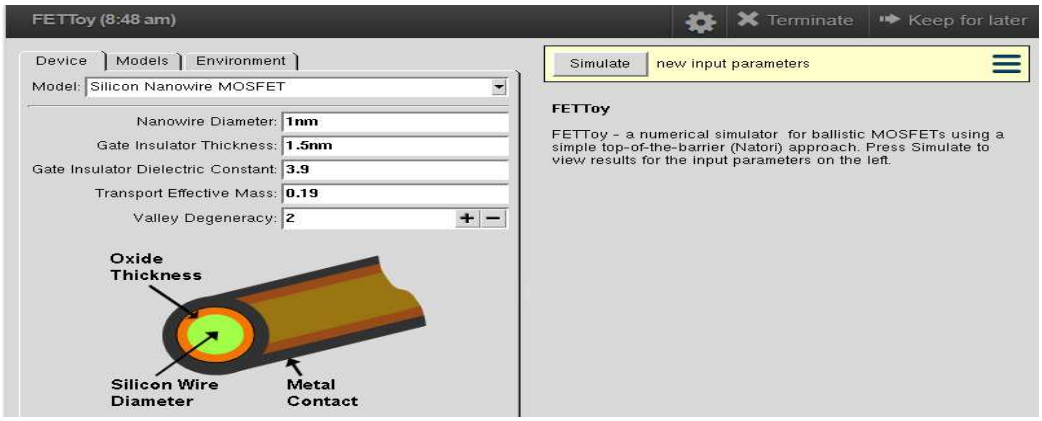

Plate 1: FETTOY Software interface

The simulating procedure was as follows;

1. Modelling of the device was done by choosing the device type (carbon nanotube and silicon nanowire gate MOSFET).
2. Setting the oxide thickness for sets of values (0.3, 0.5, 0.7, 0.9, 1.2nm), Gate voltage and Drain voltage 0-1V with other parameters fixed.
3. The program is then run to obtain results for each set of devices chosen.
4. Drain current, quantum capacitance and average velocity were obtained, and the results was analyzed for all the devices.

Table 1: Values of Input Parameters

FETTOY INPUT PARAMETERS	VALUES
Oxide Thickness	0.3-1.2 (nm)
Insulator dielectric constant	3.9
Temperature	300 (K)
Initial gate voltage	0 (V)
Final gate voltage	1 (V)
Number of bias points (gate)	13
Initial drain voltage	0 (V)
Final drain voltage	1 (V)
Number of bias points (drain)	13
threshold voltage	0.32
Gate control parameter	0.88
Drain control parameter	0.035
Series Resistance	0 (ohms)
Doping Density	1e+26 (/m^3)
Si Body Thickness	1e-08 (m)
Transport Effective Mass	0.19
Valley Degeneracy	2
Diameter	1.0nm

RESULTS AND DISCUSSION

In silicon MOSFETs, the gate oxide thickness has been consistently scaled down to maintain the field in the channel and therefore device operation at smaller channel lengths. For all devices, the effect of the gate oxide thickness scaling was analyzed. It was observed that larger oxide thicknesses cause a lowering of the saturation current and transconductance, which will impair transistor performance. With conventional silicon MOSFETs, the saturation current would be expected to scale linearly with the inverse of the oxide thickness. While some devices still rely on easily formed, relatively thick oxide layers, it can easily be seen that a primary goal in transistor design should be minimizing the oxide thickness while maintaining charge in the channel appropriate for transistor operation. At low gate voltages, the transistor is in its off state and very little current flows in response to a drain voltage V_d. Beyond a certain gate voltage, called the threshold voltage V_{th}, the transistor is turned on and the ON- current increases with increasing gate voltage V_g.

Drain current (I_d) against gate voltage (V_g)

Figures7-10, show the simulation results of CNT and SNW MOSFETs devices respectively in determining the drain current at different gate voltage, oxide thickness (0.3, 0.5, 0.7, 0.9, 1.2 nm) and at a constant drain voltage of 1V with diameter 1.0 nm.

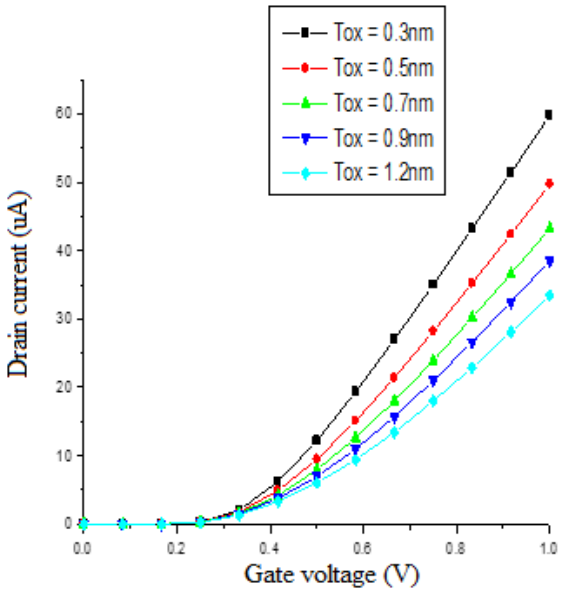

Figure 3. Graph of drain current against gate voltage for different oxide thickness in carbon nanotube MOSFET

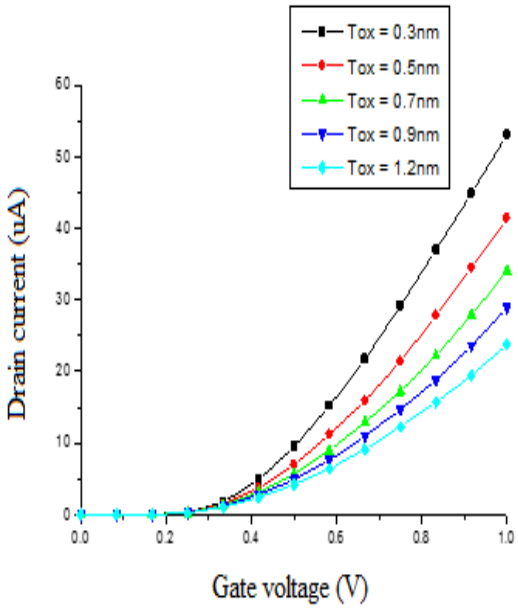

Figure 4. Graph of drain current against gate voltage for different oxide thickness in silicon nanowire MOSFET

It has been observed from Figures 3-4, that the drain current of all devices increases with the reduction in oxide thickness (T_{ox}). This means that when reducing the oxide thickness, the current capability of all devices enhances. When comparing the channel materials of CNT and SNW MOSFET, the drain current of CNT is higher at oxide thickness 0.3nm. We can conclude that the conductivity of the carbon nanotube MOSFET is inversely proportional to the oxide thickness.

Quantum capacitance (QC) versus gate voltage (V_g)

Figures 5-6 show the simulation results of CNT and SNW MOSFETs devices respectively in determining the quantum capacitance at different gate voltage, oxide thickness (0.3, 0.5, 0.7, 0.9, 1.2 nm) and at a constant drain voltage of 1V with diameter 1.0 nm.

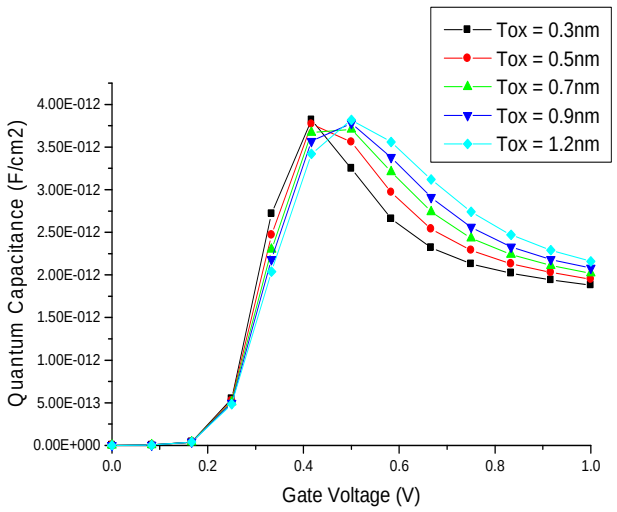

Figure 5: A graph of quantum capacitance against gate voltage for different oxide thickness in carbon nanotube MOSFET

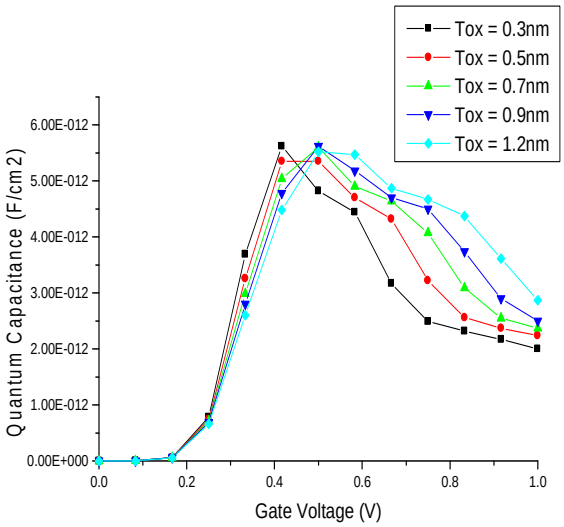

Figure 6: A graph of quantum capacitance against gate voltage for different oxide thickness in silicon nanowire MOSFET

It has been observed from Figures 5-6, at low gate voltage of 0.166 volts, the quantum capacitance of $CNT = 0.039pF$ and $SNW = 0.059pF$ for oxide thickness 0.3nm. However, it is clear from Figure 5, that as the gate voltage increased above 0.5V it shows a dropping trend, i.e., quantum capacitance decreases with decrease in oxide thickness in carbon nanotube MOSFET devices. A device can be operated at quantum capacitance limit when its gate capacitance is considerably higher than quantum capacitance (Rakesh, 2013) govern by the equation $C_g = Q/V_g$. We can conclude that the effect of quantum capacitances is quite prominent in the case of carbon nanotube and silicon nanowire MOSFET devices, which effectively reduces the gate capacitance as compare to single gate and double gate nano MOSFET devices (Galadanci et al., 2018).

Average velocity mobile electron versus gate voltage (V_g)

Figures7-8, show the simulation results of CNT and SNW MOSFETs devices respectively in determining the quantum capacitance at different gate voltage, oxide thickness (0.3, 0.5, 0.7, 0.9, 1.2 nm) and at a constant drain voltage of 1V with diameter 1.0 nm.

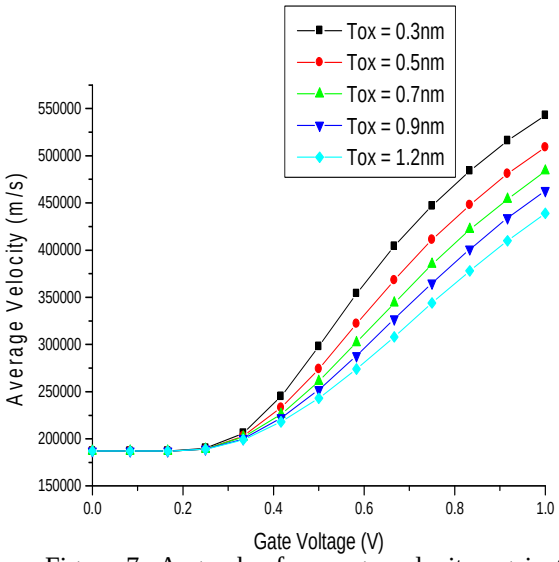

Figure 7: A graph of average velocity against gate voltage for different oxide thickness in carbon nanotube MOSFET

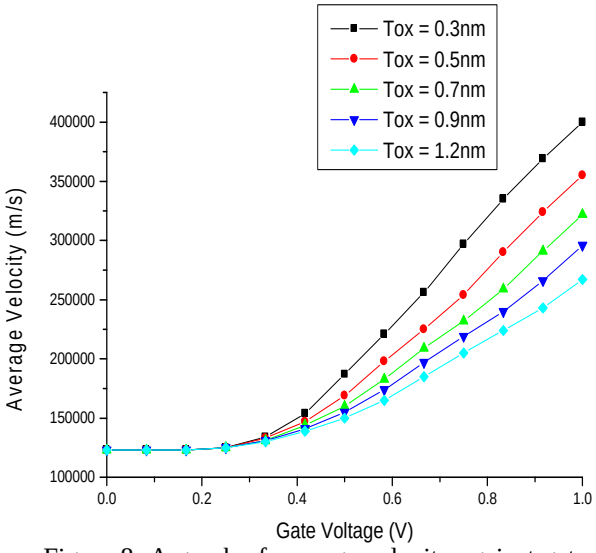

Figure 8: A graph of average velocity against gate voltage for different oxide thickness in silicon nanowire MOSFET

It has been observed from Figures 7-8, that as oxide thickness goes down from 1.2 to 0.3nm the average velocity of mobile electron for both carbon nanotube and silicon nanowire increases when we apply a gate voltage of 0.33V and above. We can conclude that carbon nanotube at oxide thickness of 0.3nm with constant drain voltage of 1V has higher average velocity of electron with no effect on the oxide thickness.

Comparison of results analysis

Various comparative study of electrical properties of carbon nanotube and silicon nanowire MOSFETs has been analyzed with FETTOY simulating software. The variation of higher transconductance, higher conductance, carrier injection velocity, on current (Ion), subthreshold swing and drain induced barrier lowering were also obtained at different oxide thickness.

Table 2-3 shows the output simulation results of carbon nanotube and silicon nanowire MOSFET devices at the highest transconductance (gm) and highest conductance (gd) for different oxide thickness.

Table 2: Variation of transconductance (gm) with different channel materials at various oxide thickness

Oxide thickness	Tox = 0.3nm	Tox = 0.5nm	Tox = 0.7nm	Tox = 0.9nm	Tox = 1.2nm
CNT	1.00E-04	8.76E-05	7.89E-05	7.23E-05	6.49E-05
SNW	9.78E-05	8.29E-05	7.31E-05	6.46E-05	5.25E-05

Table 3: Variation of conductance (gd) with different channel materials at various oxide thickness

Oxide thickness	Tox = 0.3nm	Tox = 0.5nm	Tox = 0.7nm	Tox = 0.9nm	Tox = 1.2nm
CNT	4.00E-06	3.51E-06	3.16E-06	2.91E-06	2.62E-06
SNW	3.93E-06	3.33E-06	2.95E-06	2.65E-06	2.23E-06

It has been observed from Table 2-3 that as oxide thickness goes down from 1.2 to 0.3nm the transconductance (gm) and conductance (gd) for all devices increases. We can conclude that carbon nanotube has the highest transconductance (gm) and conductance (gd) at oxide thickness of 0.3nm.

Table 4-5 shows the output simulation results of carbon nanotube and silicon nanowire MOSFET devices at carrier injection velocity (v_inj) and on current (Ion) at oxide thickness for different oxide thickness.

Table 4: Variation of carrier injection velocity (v_inj) with different channel materials at various oxide thickness

Oxide thickness	Tox = 0.3nm	Tox = 0.5nm	Tox = 0.7nm	Tox = 0.9nm	Tox = 1.2nm
CNT	5.43E+05	5.09E+05	4.84E+05	4.63E+05	4.40E+05
SNW	4.00E+05	3.55E+05	3.22E+05	2.96E+05	2.67E+05

Table 5: Variation of on current (Ion) with different channel materials at various oxide thickness

Oxide thickness	Tox = 0.3nm	Tox = 0.5nm	Tox = 0.7nm	Tox = 0.9nm	Tox = 1.2nm
CNT	5.98E-05	4.97E-05	4.32E-05	3.85E-05	3.35E-05
SNW	5.31E-05	4.14E-05	3.40E-05	2.89E-05	2.38E-05

It has been observed from Table 4-5 that as oxide thickness goes down from 1.2 to 0.3nm the carrier injection velocity (v_inj) and on current (Ion) for both carbon nanotube and silicon nanowire increases. We can conclude that carbon nanotube has the highest carrier injection velocity (v_inj) and on current (Ion) at oxide thickness of 0.3nm.

Table 6-7 shows the output simulation results of carbon nanotube, silicon nanowire, single gate and double gate MOSFET devices for subthreshold (S) and drain induced barrier lowering (DIBL) at different oxide thickness.

Table 6: Variation of subthreshold with different channel materials at various oxide thickness

Oxide thickness	Tox = 0.3nm	Tox = 0.5nm	Tox = 0.7nm	Tox = 0.9nm	Tox = 1.2nm
CNT	67.84	67.80	67.70	67.70	67.70
SNW	67.84	67.65	67.63	67.66	67.69

Table 7: Variation of DIBL with different channel materials at various oxide thickness

Oxide thickness	Tox = 0.3nm	Tox = 0.5nm	Tox = 0.7nm	Tox = 0.9nm	Tox = 1.2nm
CNT	39.70	41.10	41.10	41.10	41.10
SNW	41.00	41.10	41.20	41.20	41.20

It has been observed from Table 6-7 that as oxide thickness goes down from 1.2 to 0.3nm the subthreshold (S) and drain induced barrier lowering for for both carbon nanotube and silicon nanowire decreases. We can conclude that carbon nanotube has lower drain induced barrier lowering at oxide thickness of 0.3nm.

CONCLUSION

In this work, we have observed comparative study of electrical properties of carbon nanotube and silicon nanowire MOSFET devices on drain current, quantum capacitance and average velocity of mobile electron by the variation of oxide thickness for set of value (0.3nm, 0.5nm, 0.7nm, 0.9nm and 1.2nm) at different gate voltage through an extensive simulating software (FETTOY) obtain online from nanohub.org. The results obtained were compared and analyzed, through the results shown in Figures 3-8 and Table 2-7, we can conclude that in deep nanometer regime carbon nanotube has highest transconductance (g_m) of 1.00×10^{-4}S, highest conductance (g_d) of 4.00×10^{-6}S, highest carrier injection velocity (v_{inj}) of 5.43×10^5m/s, highest on current (Ion) of 59.79μA, at oxide thickness of 0.3nm when used as MOSFET device. Highest transconductance and highest carrier injection velocity means gate has more control over the charge in the channel materials and the mobility of charge carrier in these channel materials is higher respectively.

Finally, Carbon nanotube has subthreshold swing (S) of 67.79 mV/dec, drain induced barrier lowering (DIBL) of 39.67 mV/V, lesser quantum capacitance to improve propagation delay, reduced leakage current, as well as maximum carrier mobility. It shows better performance than silicon nanowire MOSFET devices.

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